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GATED HIGH SPEED OPTICAL DETECTOR

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16. Abstract

The objective of this program was to design, fabricate, test, and deliver two gated high speed optical detectors for use in high speed digital laser communication links at NASA GSFC and Army ECOM. The optical detectors utilized a dynamic crossed field photomultiplier and electronics including dc bias and RF drive circuits, automatic remote synchronization circuits, automatic gain control circuits, and threshold detection circuits. The NASA equipment will be used in laboratory and field experiments to detect 400 Mbps binary encoded signals from a mode locked Nd:YAG laser transmitter at the fundamental 1.06 μm wavelength or the doubled 0.53 μm wavelength by means of interchangeable photomultiplier heads. The ECOM equipment will operate at 200 Mbps and is supplied only with a 1.06 μm head. The NASA equipment only included a set of error rate measurement electronics. Detailed test data on both sets of equipment was made.

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CONTENTS

CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

Figures Page

LIST OF TABLES

GATED HIGH SPEED OPTICAL DETECTOR

1. INTRODUCTION

The gated high speed optical detectors which were fabricated, tested, and delivered under this program include a 400 Mbps receiver for NASA GSFC and a 200 Mbps receiver for Army ECOM. The NASA receiver is operable at 0.53 μm and 1.06 μm by means of interchangeable detector heads. The ECOM receiver is supplied only with a 1.06 μm detector head. The equipment functions as a gated high speed photomultiplier receiver for pulsed, binary encoded, laser radiation. The NASA receiver is described in sections 1 through 6. The ECOM receiver is described in section 7.

The Optical Detector is comprised of a detector power supply and control unit, electronics module stack and optical detector head. It performs optical detection, electron amplification, gating, threshold detection, gain control, and remote synchronization, and includes all power supplies. The first three functions are performed by a dynamic crossed field photomultiplier (DCFP) in the detector head; the remainder by electronic circuits.

A simplified block diagram of the Optical Detector is shown in Figure 1. Incoming pulsed laser radiation incident on the DCFP photocathode yields photoelectrons which are amplified by secondary emission multiplication on the DCFP dynodes. The sensitivity of the receiver to low laser light levels is a function of the photocathode quantum efficiency and the secondary multiplication gain. The DCFP internal gating can significantly reduce the effect of background radiation. Receiver gating is synchronized with the incoming optical signal pulse train by means of a unique dithered gate phase discriminator phase locked loop. An AGC loop is used to maintain the output level nearly constant over the allowed input signal level range. The DCFP output is amplified and threshold detected to recover the original binary modulation on the laser beam. The data output is converted to NRZ format. Photos of the equipment are presented in Figures 2, 3, and 4.

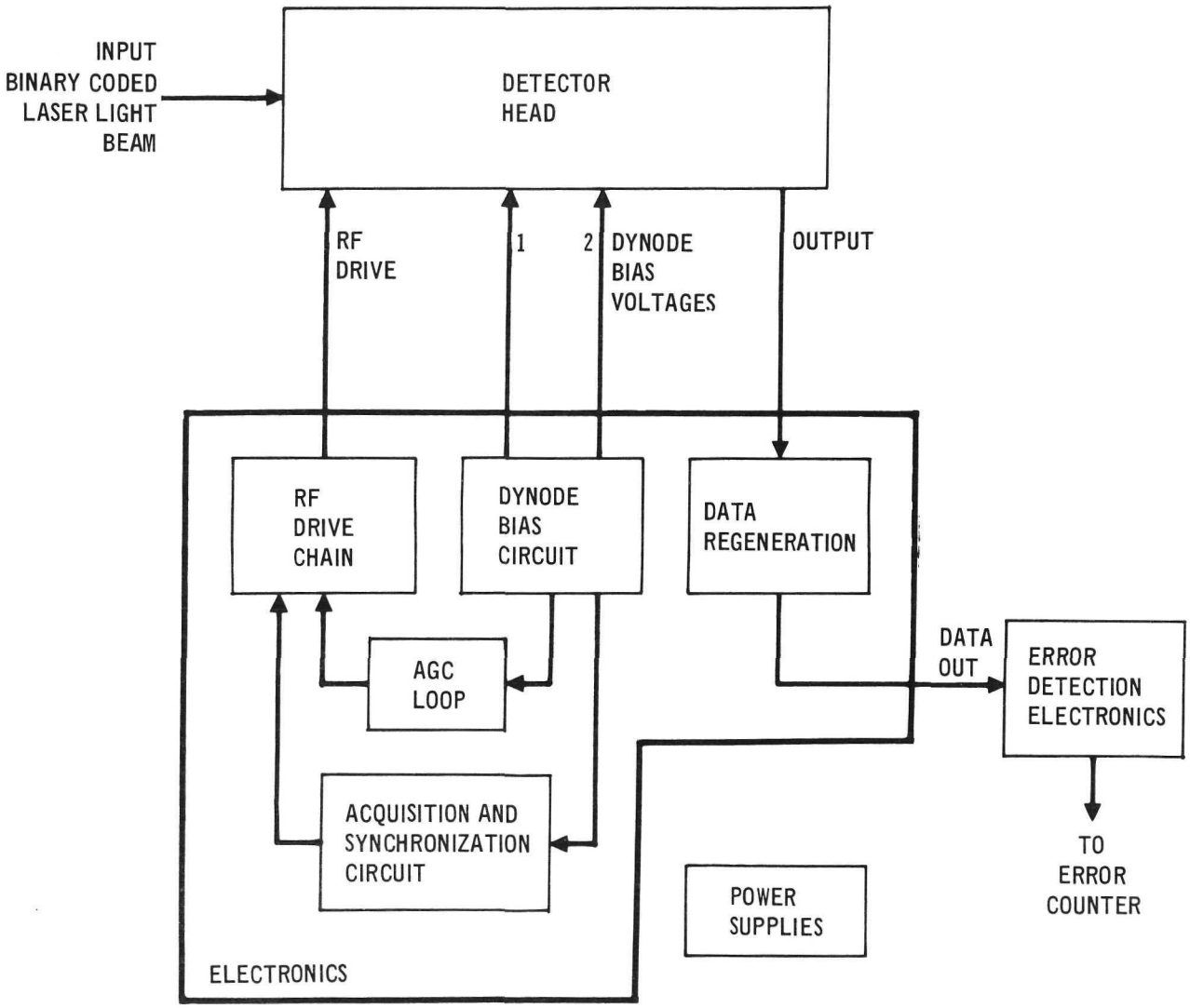


FIGURE 1 SIMPLIFIED BLOCK DIAGRAM OF OPTICAL DETECTOR

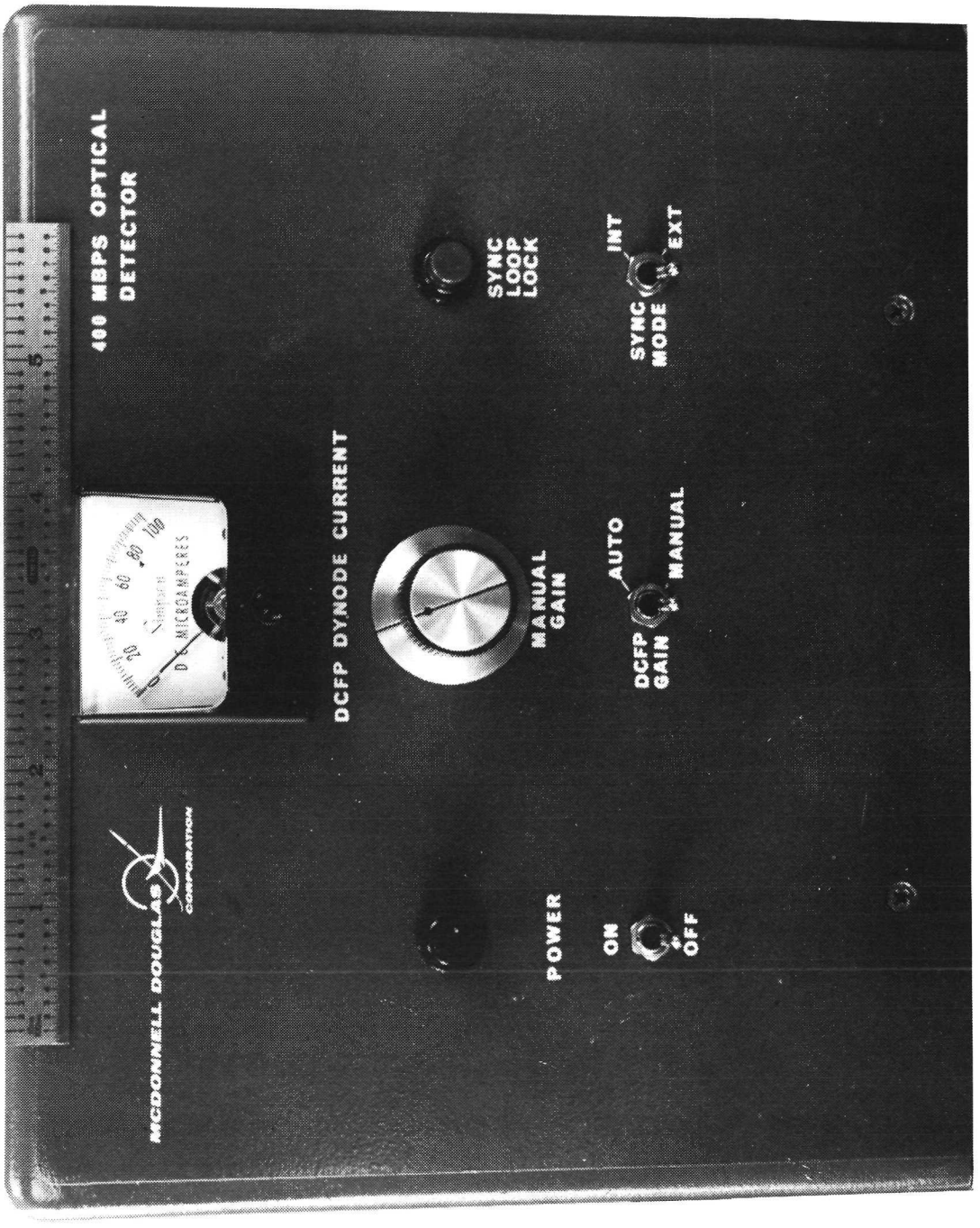


FIGURE 2 POWER SUPPLY AND CONTROL UNIT

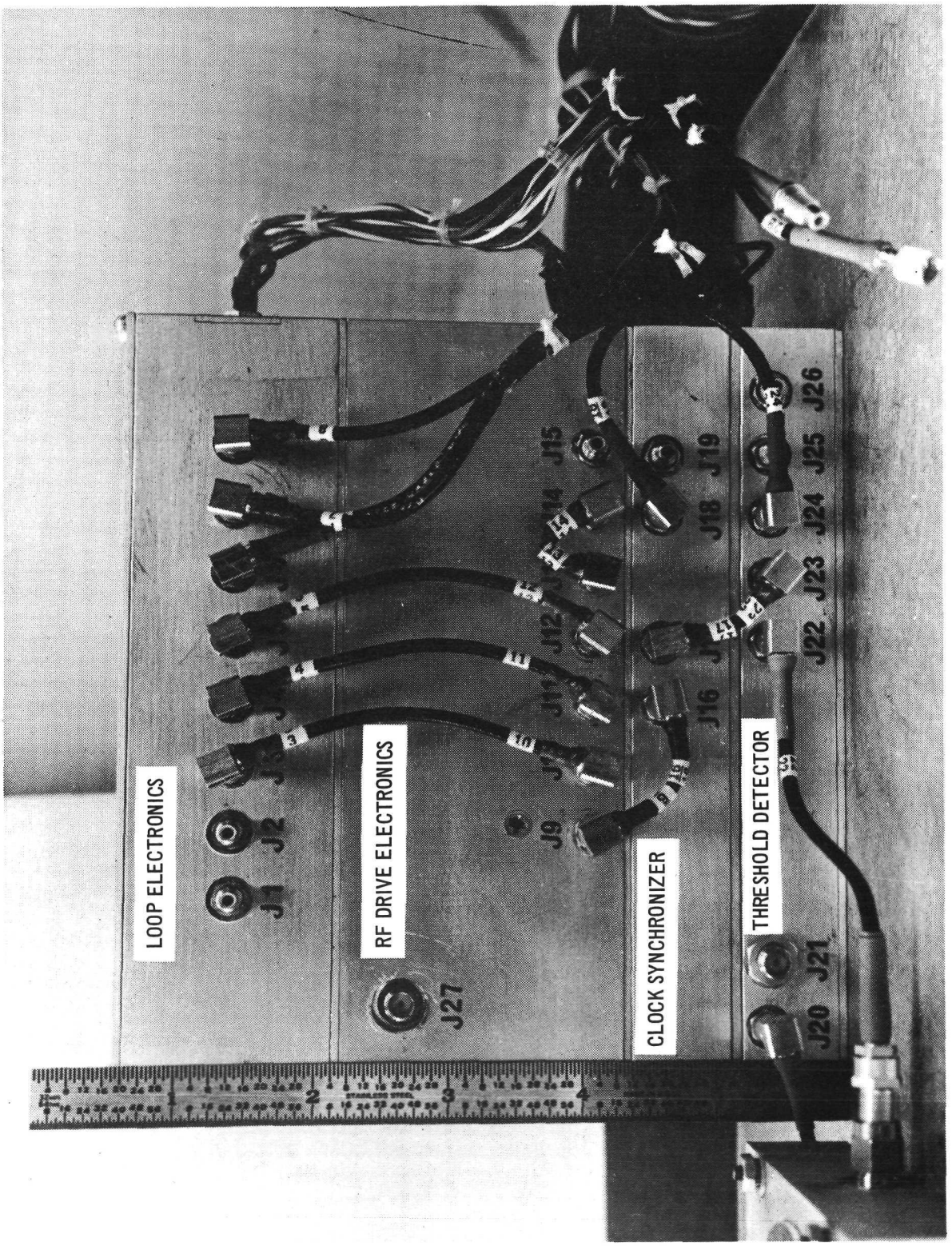


FIGURE 3 RECEIVER ELECTRONICS MODULE STACK

FIGURE 4 OPTICAL DETECTOR ASSEMBLY

The NASA Optical Detector only is accompanied by a set of error rate electronics shown in Figure 5. The error rate electronics compare the optical detector output with the original transmitted code and determine when errors occur. Experimental communication system error rate measurements were made using a 400 Mpps mode locked and frequency doubled Nd:YAG laser modulated by a 400 Mbps pseudorandom code in conjunction with the 400 Mbps gated high speed optical detector and these error detection electronics.

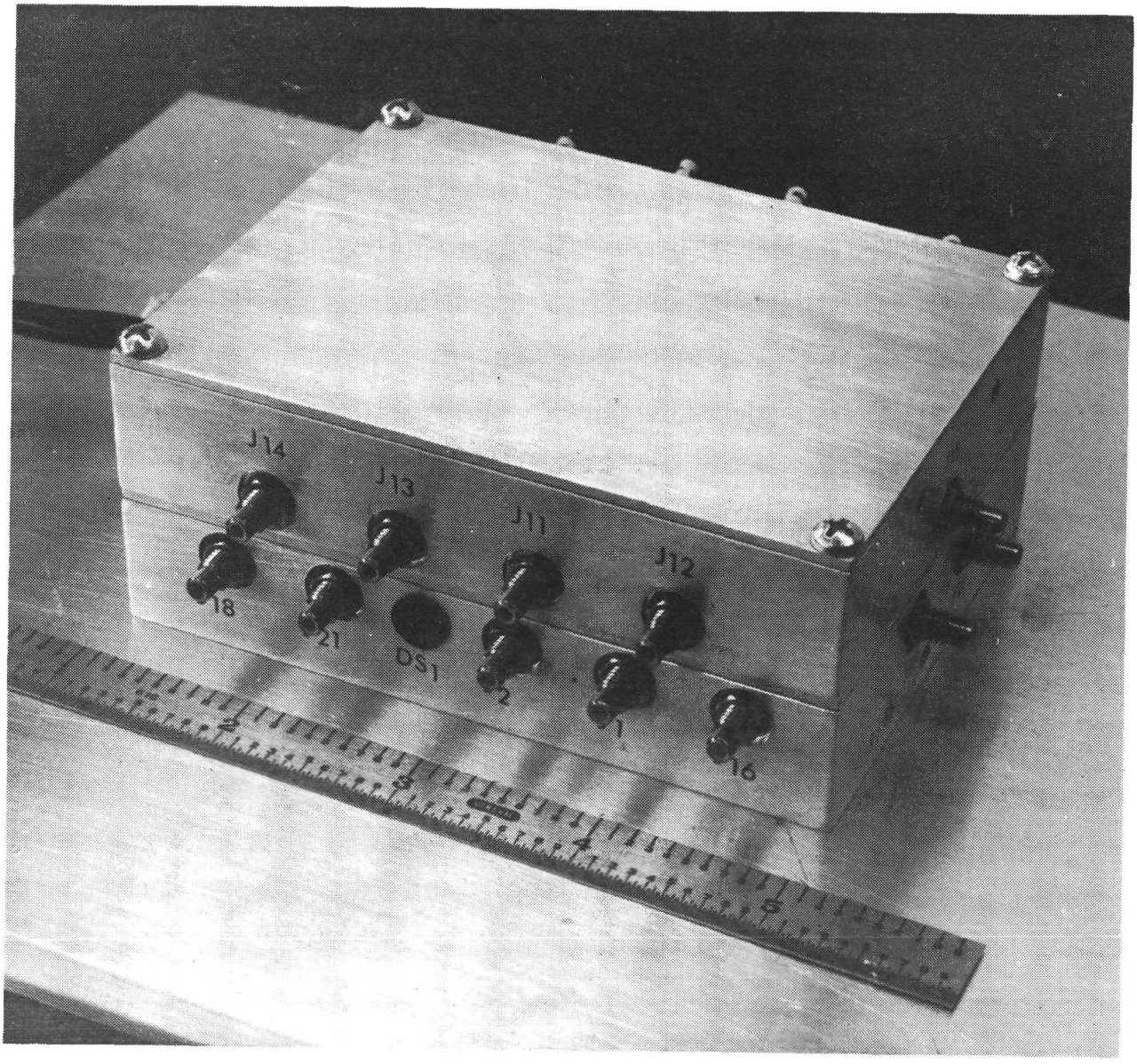


FIGURE 5 ERROR RATE ELECTRONICS

2. PERFORMANCE SUMMARY

Measured performance results on the delivered NASA 0.53 μm Optical Detector are presented in Table 1. The 1.06 μm DCFP is not available from the manufacturer at the time of this writing.

TABLE 1

SUMMARY OF PERFORMANCE RESULTS

CHARACTERISTIC USING DCFP S/N 013	Value
Operating Wavelength (micrometers)	0.53
Photocathode Quantum Efficiency (maximum)	5%
Dynamic Range of Signal Input (Photoelectrons per pulse)	30 - 1000
Required Input Laser Pulse Width	<500 picoseconds (at the 10% of maximum points)
Synchronization	
Acquisition range at 400 Mbps	± 67 kHz
Deviation rate product	>3 x 10^5 Hz/sec
Acquisition time (maximum)	1 sec
Loop bandwidth	1 kHz
Clock/Data Timing Accuracy (picoseconds)	± 50
Outputs	Two complementary outputs in NRZ format. Output levels are -800 mv and -1600 mv.

3. HARDWARE DESCRIPTION

A functional block diagram of the Optical Detector is shown in Figure 6. It is comprised of a power supply and control unit, a stack of electronic modules, and a detector head containing the DCFP, the adjustable magnetic field assembly, and protective circuit which prevents the application of RF drive power in the absence of dc dynode bias voltages. Two interchangeable detector heads are supplied, one for 0.53 μm, and one for 1.06 μm. The electronic modules perform the tasks of RF drive power generation, acquisition and synchronization, automatic gain control, threshold detection, and regeneration of received data in NRZ format. The error rate electronics serve as communications system test equipment and are packaged separately.

3.1 DETECTOR.

The function of the DCFP detector is to convert the pulsed laser signal into an electrical pulse train with sufficient amplitude to drive the post detection electronics.

The DCFP is a high speed photomultiplier which is driven by a radio frequency (RF) electric field, dc biasing fields, and a crossed static magnetic field. It offers the advantages of high gain, relatively large photocathode area, and internal subnanosecond gating. Receiver gating is useful in rejecting a portion of the extraneous background radiation by temporal discrimination. The gating recurs at a specific portion of each cycle of the RF drive frequency, so that the DCFP is particularly useful for receiving regularly recurring optical pulses from a mode-locked laser transmitter.

Detection of pulsed optical inputs is achieved in the DCFP by sampling the photoelectrons generated at the photocathode at the frequency of the RF driving field. These electron bunches are then multiplied in successive steps by means of secondary emission. The electron bunches are focused in position and phase, such that large current gains are achieved without pulse to pulse overlap. The DCFP is illustrated in Figure 7.

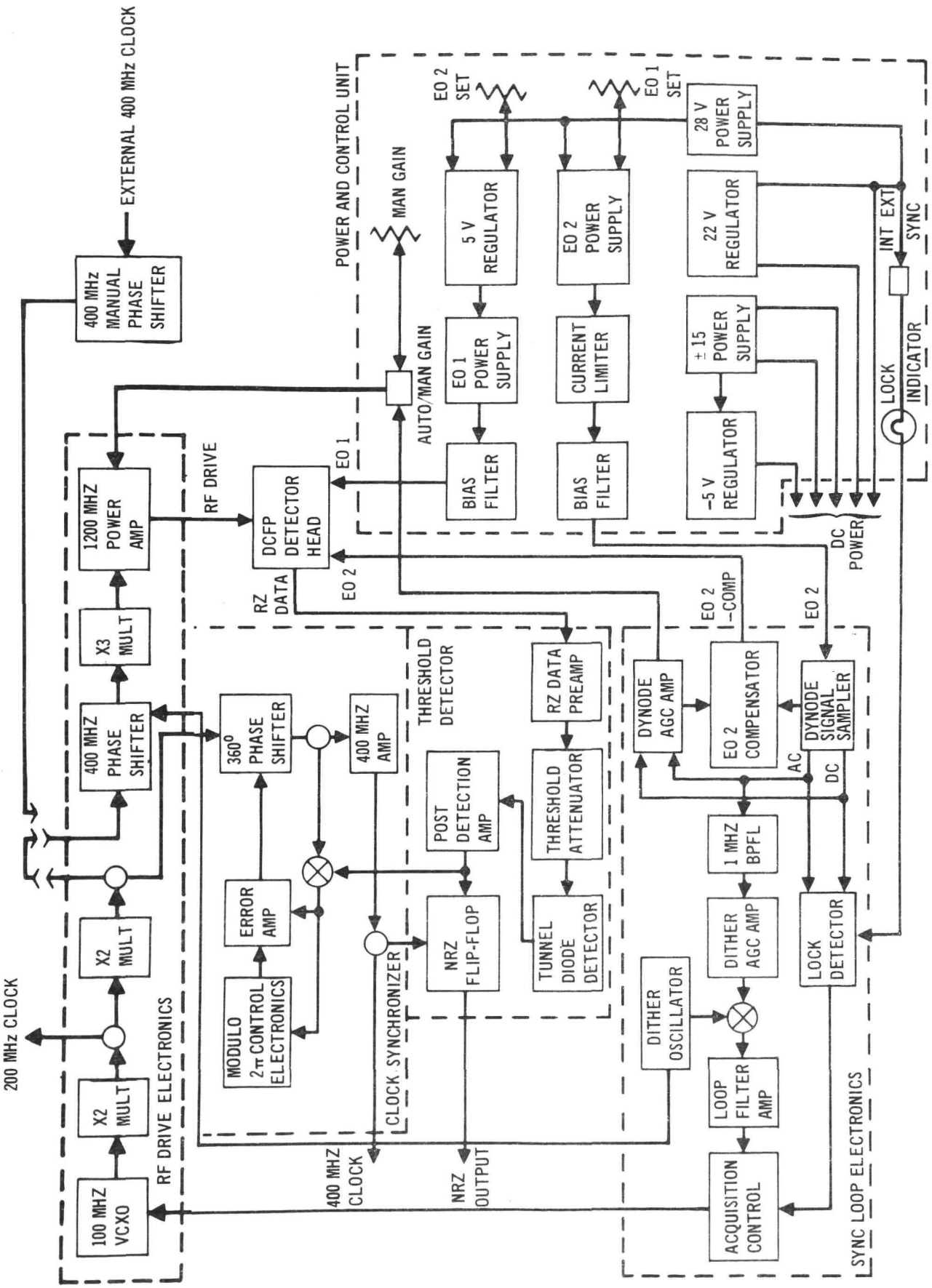


FIGURE 6 400 Mbps OPTICAL DETECTOR BLOCK DIAGRAM

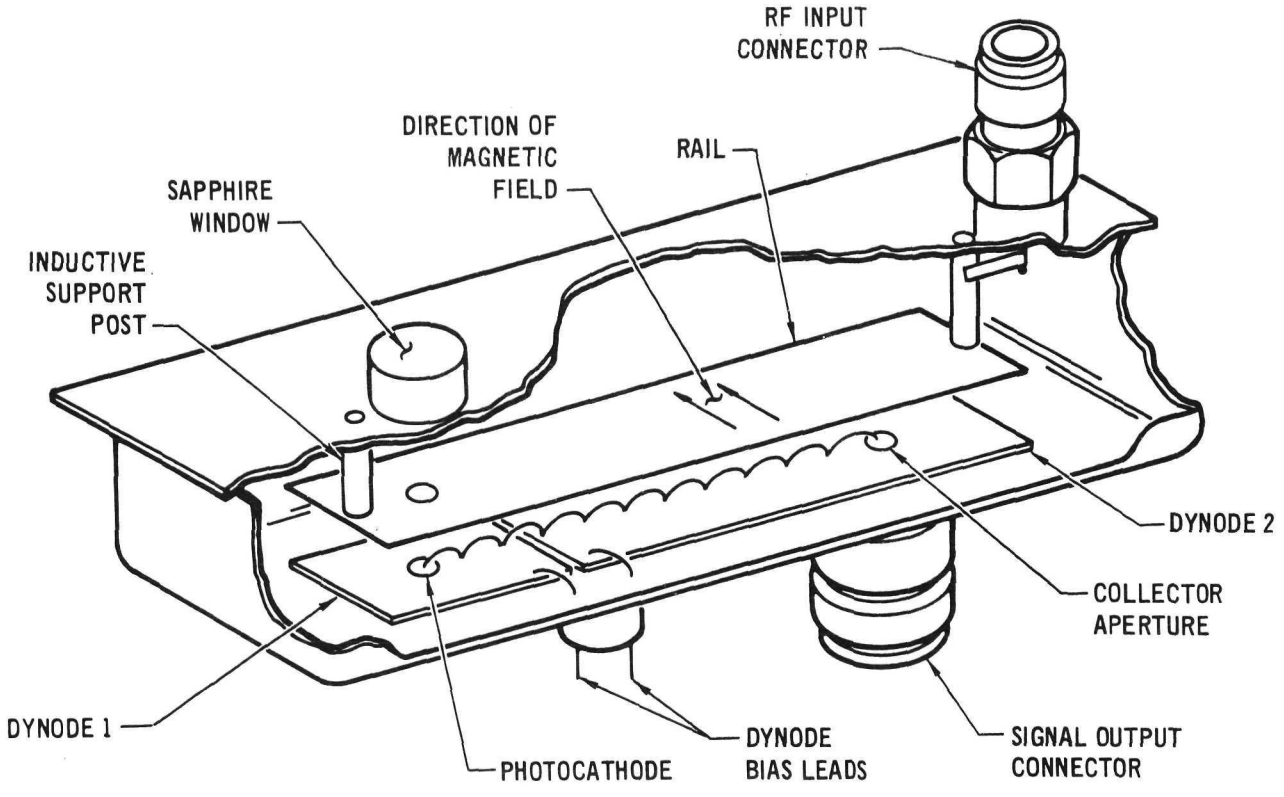


FIGURE 7 ILLUSTRATION OF DYNAMIC CROSSED FIELD PHOTOMULTIPLIER

The DCFP consists of two parallel metal strip electrodes between which is applied an RF driving electric field and a dc biasing electric field. A static magnetic field is applied normal to the electric field, and normal to the length of the strips. so that an electron in motion between the strips moves along the direction of the strips. The lower strip has a photocathode near one end, a collecting hole near the other, and is treated to be a good secondary emitting surface. Photoelectrons generated at the photocathode are accelerated towards the top strip, or rail, during the positive half cycle of the RF drive, and the magnetic field causes them to curve in a cycloidal path towards the collector end of the assembly. On the opposite half cycle, the electrons are returned to the lower strip with sufficient energy so that each electron generates several secondary electrons. The secondary electron multiplication process is repeated until reaching the collecting hole near the end of the lower strip. After passing through the collecting hole, the multiplied secondary electrons strike the collector, or anode. A cutaway photo of a 1 GHz DCFP is shown in Figure 8.

Only photoelectrons which are generated during the proper phase of the RF drive cycle are "sampled" and amplified by the phase-focusing secondary multiplication sequence; hence, the gating effect of the DCFP. Photoelectrons generated at other phases of the RF cycle are collected by the upper electrode which is biased strongly positive, or will follow a suboptimal trajectory in which they receive insufficient kinetic energy to generate secondary electrons when reaching the lower electrode. Changing the input pulse arrival time or shape does not result in an equivalent change in output pulse shape or arrival time. The output pulse occurs synchronously with the RF drive to the DCFP. Since there is no phase change in the DCFP output for a phase change of the optical input, a dithered gate tracking loop is required to keep the DCFP gate aligned with the input pulse.

The gain of the DCFP is proportional to RF drive power level. Only a slight compensation of DC bias is required as the RF drive power level is varied. This feature allows both manual and automatic control of DCFP gain.

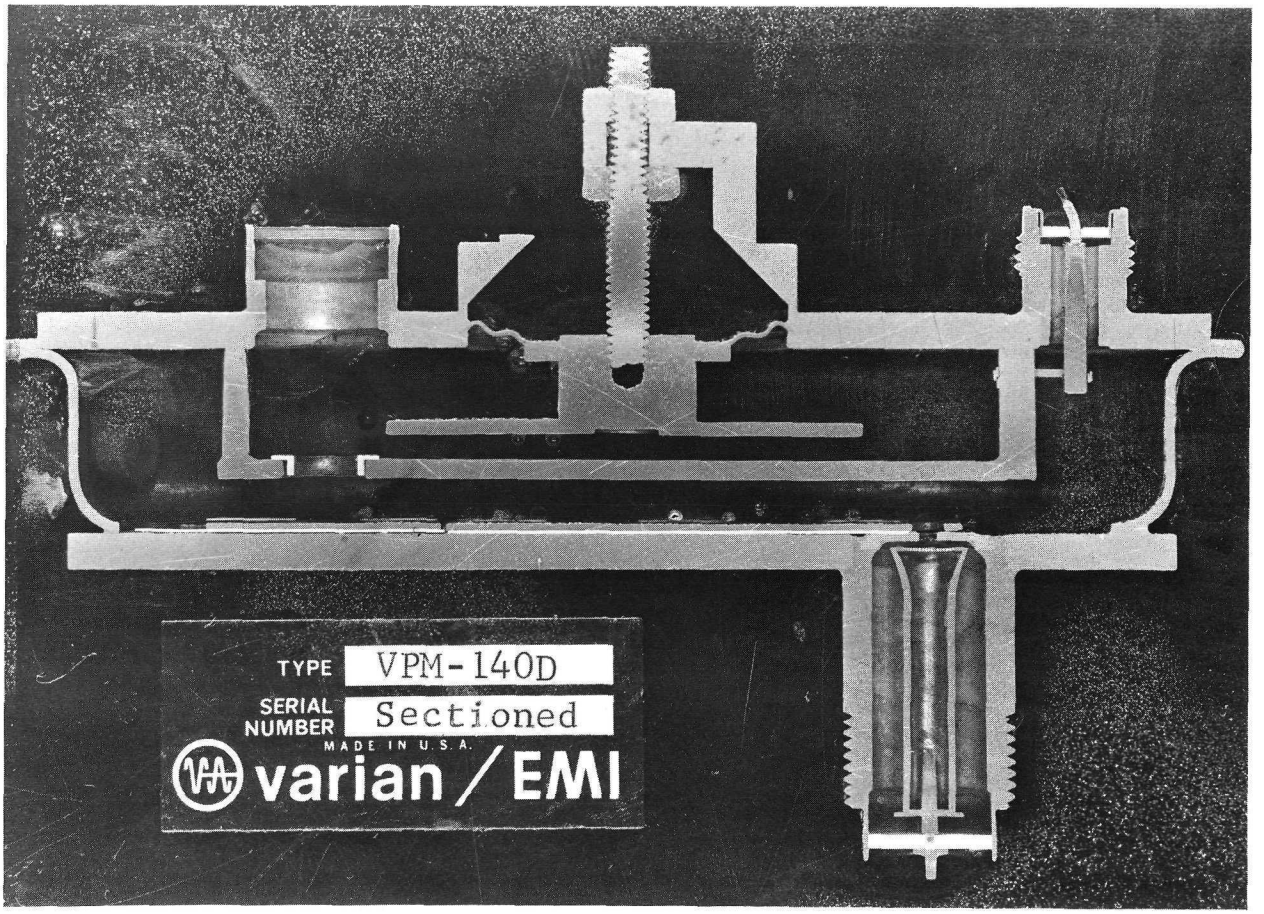


FIGURE 8 CUTAWAY VIEW OF DCFP

3.2 RF DRIVE CHAIN.

The purpose of the RF drive chain is to provide the 1.2 GHz source, with appropriate amplitude, frequency, and phase characteristics, for the DCFP tube. The output signal is modulated by control signals from other portions of the receiver in order to control the current gain of the DCFP and to implement acquisition and synchronization to the input optical pulse train.

The required 1.2 GHz drive source must be a very stable low noise RF signal. A block diagram of the RF drive chain is presented in Figure 9. The tuning range is $\pm$ 240 kHz at 1.2 GHz. The oscillator tuning rate is dc to 20 kHz. The phase of the 1.2 GHz signal is dithered 0.1 radian peak-to-peak in order to implement the dithered gate phase discriminator. DCFP gain is controlled by varying the RF drive power from 0.5 to 1.8 watts.

The fundamental frequency source is a Voltage Controlled Crystal Oscillator (VCXO). Its 100 MHz output is amplified, frequency doubled, and filtered. A portion is sampled by a power divider to provide an external 200 MHz signal in addition to the required internal signal. The 200 MHz signal is then frequency doubled, filtered, and split to provide two 400 MHz outputs. One 400 MHz output is then fed to the clock synchronizer while the other is fed back into the RF chain with an external jumper. An external 400 MHz source is used in place of this internally generated 400 MHz signal in the external synch mode. The 400 MHz signal is then "phase dithered", amplified, frequency tripled, filtered, and amplified to produce the high level 1.2 GHz signal. The final amplifier has a gain control input to electronically set the power output level. The 1.2 GHz output drives the DCFP and supplies the energy for the secondary multiplication process.

3.3 SYNCHRONIZATION LOOP ELECTRONICS.

Synchronization of the DCFP gate with the incoming optical pulse train is achieved by the synchronization loop electronics. A functional diagram of the synchronization circuitry is shown in Figure 10. A 1.0 MHz crystal oscillator is the dither signal source. This dither signal phase modulates the DCFP RF drive signal and causes the gate to alternately advance and retard

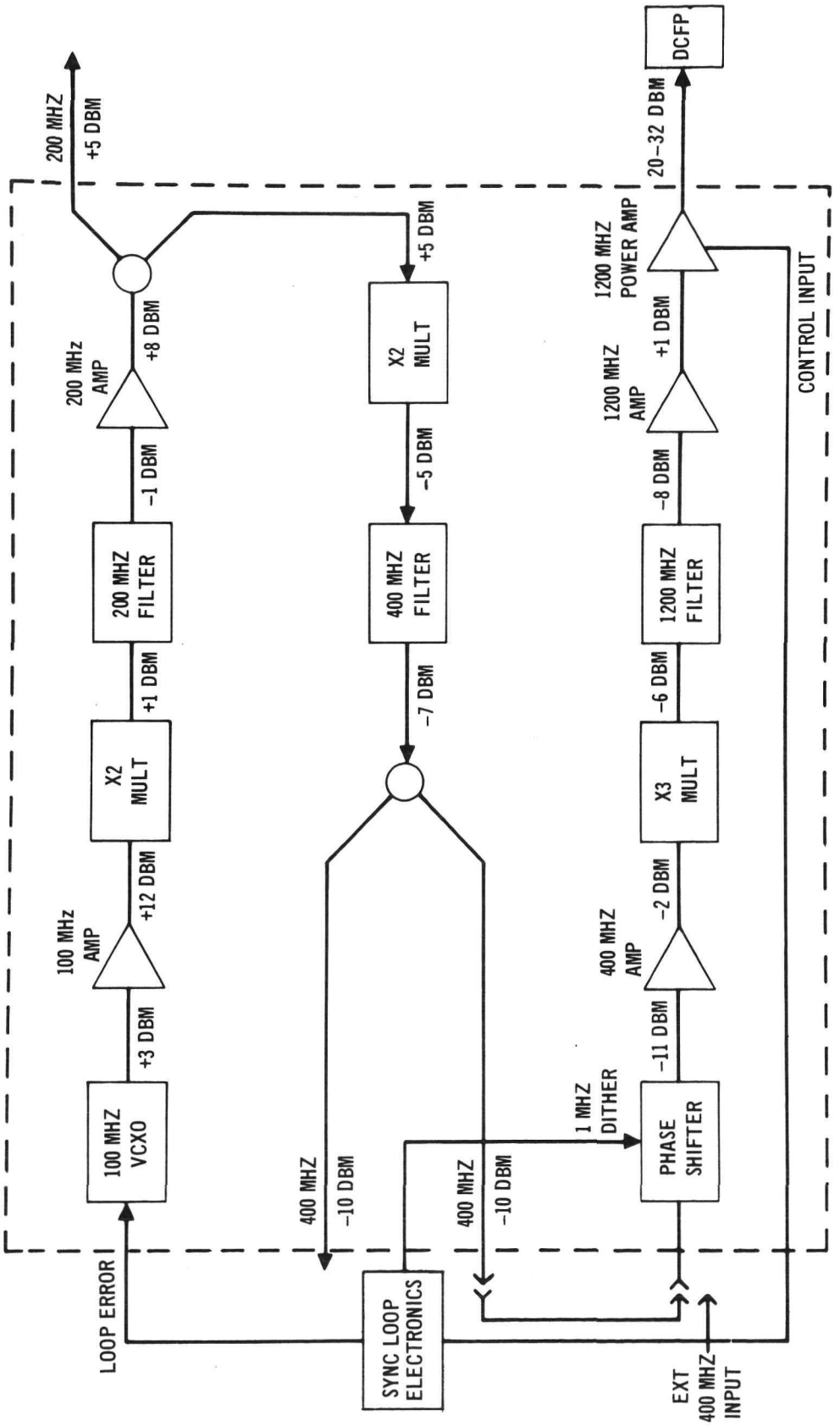


FIGURE 9 RF DRIVE ELECTRONICS FUNCTIONAL DIAGRAM (NASA)

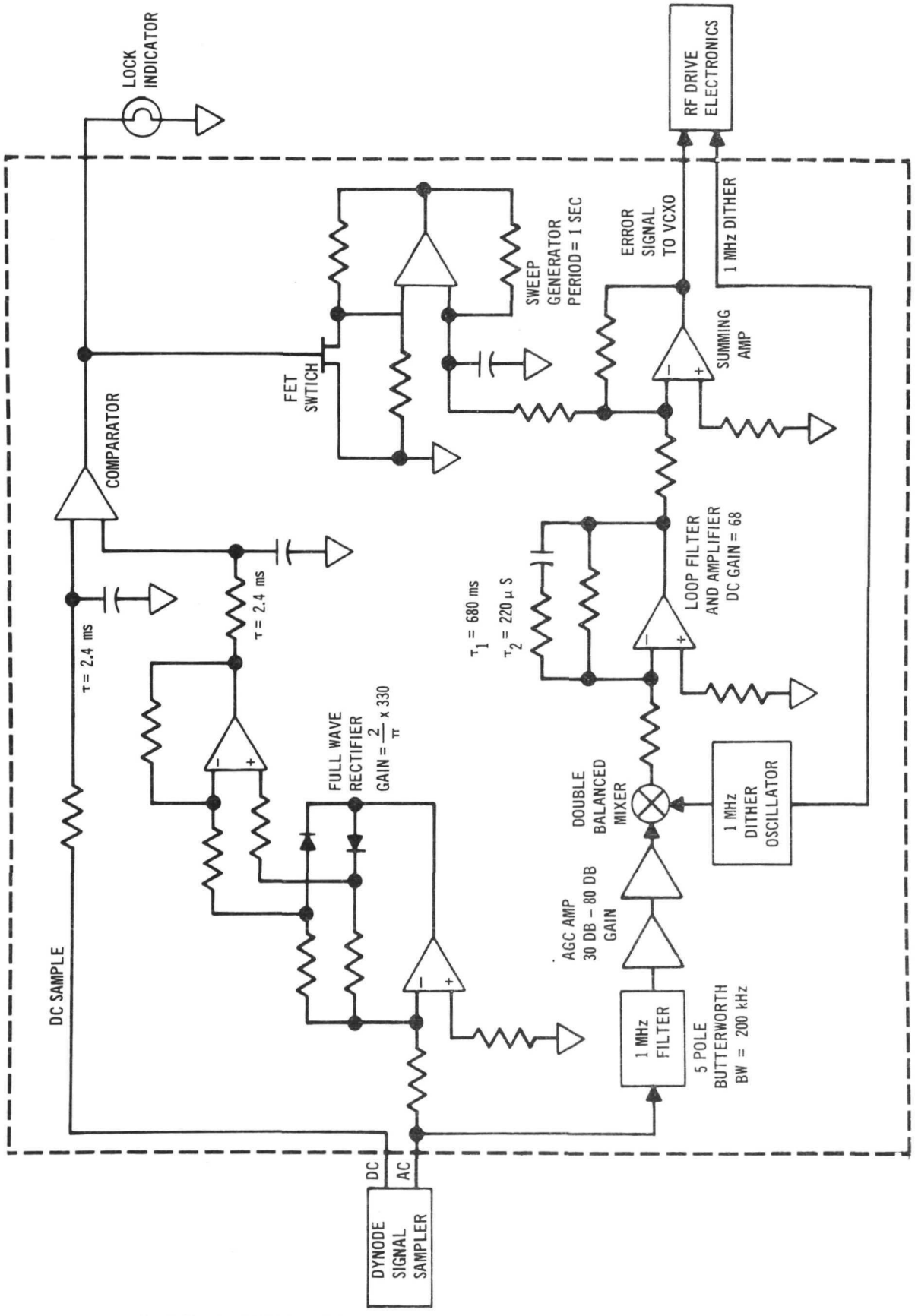


FIGURE 10 SYNC LOOP ELECTRONICS FUNCTIONAL DIAGRAM

with respect to the optical pulse train. This process produces a 1 MHz component at the DCFP output which is in phase or out of phase with the dither signal depending on whether the gate precedes or follows the optical pulse. This dither frequency signal component is sampled at the 2nd dynode. The phase and amplitude of the recovered dither signal depend upon the relative timing error between the gate and pulse positions. The recovered dither frequency signal is then filtered to eliminate harmonics and beat frequency signals, and amplified by an AGC amplifier. The magnitude of the recovered dither frequency signal component is dependent upon the magitude of the RF carrier phase deviation, the average 2nd dynode current, the gating characteristics of the DCFP, and the width of the input optical signal pulse. Typically, for 0.1 radians peak-to-peak deviation and 0.3ma dynode current, this signal level is 0.3 mV. The AGC amplifier output level to the mixer remains constant at approximately 500 mV and thus normalizes the loop gain for all operating conditions.

The double balanced mixer is used as a phase detector which produces an error voltage proportional to the phase difference between the recovered dither component and a reference signal from the dither oscillator. The loop filter is a conventional lead-lag network producing a natural loop frequency of $\omega_n = 6.28 \times 10^3$ rad/sec and a damping factor of 0.7. The summing amplifier adds the error signal and a triangular sweep voltage which is enabled when the receiver is not synchronized. This composite error signal controls the phase and frequency of the 100 MHz VCXO in the RF drive electronics which in turn controls the phase and frequency of the DCFP RF drive signal.

The lock detector determines whether the loop is locked, controls the operation of the acquisition sweep generator, and also provides a signal to light the remote lock indicator. When the loop is not locked, a beat note is present at the dynode at the difference frequency between the optical pulse train and the RF drive frequency. A fullwave rectifier with an overall gain of about 200 produces a sufficiently large signal at the comparator to switch it, when a beat note is detected. When the loop locks, the beat note disappears and the comparator switches to the locked state, after a suitable holding time determined by the input RC network.

3.4 AUTOMATIC GAIN CONTROL.

The function of the automatic gain control (AGC) and bias compensation circuitry is to provide a constant output pulse amplitude to the threshold decision circuits.

The secondary multiplication current gain of the DCFP is proportional to the applied RF drive power. Thus the DCFP is well suited to automatic gain control. Performance does not deteriorate over a wide range of applied RF drive power. However, a slight change in step size occurs with changes in RF electric field, thereby requiring a small tracking correction in dc bias in order that the last step passes through the center of the dynode aperture to reach the anode. This correction is considered a vernier control with the primary gain control being variation in RF drive power.

The AGC and bias compensation circuits are shown functionally in Figure 11. The average dynode current is sensed by a resistor in series with the 2nd dynode bias return line. The sensed dc voltage is amplified in two cascaded operational amplifiers. The second of these provides a frequency rolloff with a time constant of 1 ms. The amplified voltage is then used to control the output power of the 1200 MHz power amplifier, which in turn controls the DCFP gain and the DCFP second dynode current, closing the loop. The anode output current is directly proportional to the 2nd dynode current.

The AGC control voltage to the power amplifier is related to the RF field and is also used to control the bias compensator. The bias compensator consists of a variable gain operational amplifier and a series pass transistor in the return side of the 2nd dynode bias supply. The series pass transistor acts as a voltage source subtracting from the bias supply some value from 1 to 25 volts. The ac component of the dynode signal is capacitively coupled from the high side of the bias supply to the synchronization loop electronics. A portion is also used in the AGC loop to extend its bandwidth and improve the phase margin.

3.5 THRESHOLD DETECTOR.

The threshold detector provides wideband amplification of the DCFP output pulse train, binary decision of the serial data on the basis of pulse amplitude,

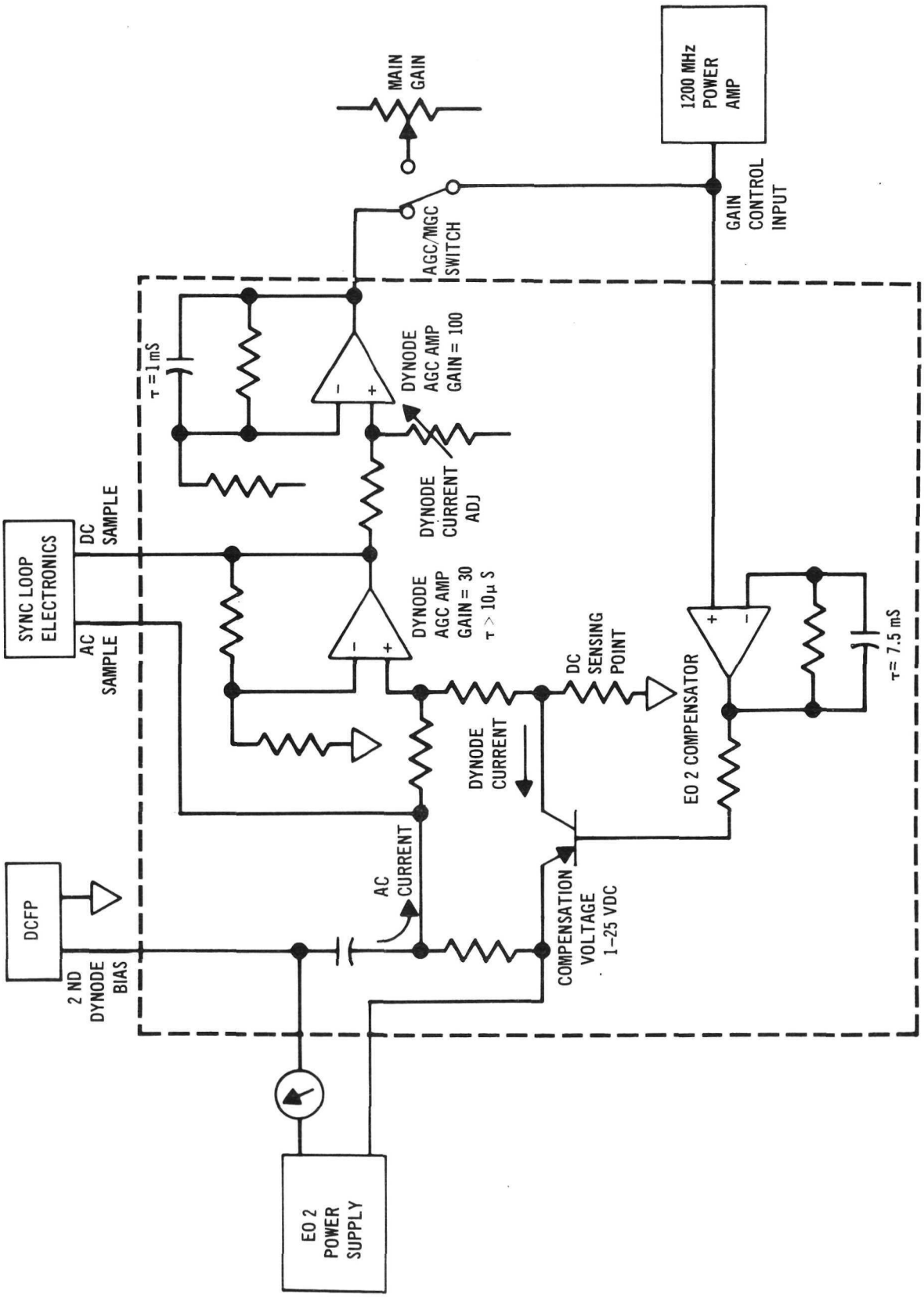


FIGURE 11 DYNODE AGC AND BIAS COMPENSATION FUNCTIONAL DIAGRAM

and conversion from return-to-zero (RZ) to a non-return-to-zero (NRZ) format. A functional diagram of the threshold detector is shown in Figure 12.

The data preamplifier has an overall gain of 100 from dc to 600 MHz. This wideband operation is achieved by combining two cascaded ac coupled hybird amplifiers with an operational dc amplifier having suitable input and output matching networks. The effective gain to the narrow DCFP output pulse is a factor of 2 to 3 less, due to the spectral components above 600 MHz.

The threshold decision is made by a tunnel diode monostable which is biased into the unstable state when a "one" level signal is present. The threshold attenuator controls the amplitude of the RZ data pulse train to the tunnel diode. The amplitude is set so that "ones" trigger the tunnel diode, but "zeros" do not.

The post detection amplifier is similar to the preamplifier with a gain of 10. The output of this amplifier is at MECL levels of -800 mV and -1600 mV. The RZ to NRZ conversion is accomplished by a D-type flip-flop. The flip-flop is clocked at a 400 MHz rate to recover the data in NRZ format. An emitter coupled pair and two emitter followers provide complementary outputs.

3.6 CLOCK SYNCHRONIZER.

The 400 MHz clock synchronizer shown functionally in Figure 13 maintains the clock signal and the data signal in a fixed phase relationship. A narrow range of relative phase shift between the clock and data signals is required for proper operation of the RZ to NRZ conversion flip-flop. Two mechanisms lead to clock/data phase variations. The first is the phase ambiguity resulting from using a 1200 MHz DCFP in a 400 Mbps system. When the synchronization loop acquires lock, the data is equally likely to appear in any one of the three possible gating sequences. The 400 MHz clock signal from the RF drive chain has three possible phase states, with respect to the data stream, that are 120° apart. The second source of phase shift is the 1200 MHz power amplifier. As the RF drive level is varied to control the DCFP gain, the phase shift through the amplifier changes leading to further clock/data uncertainty.

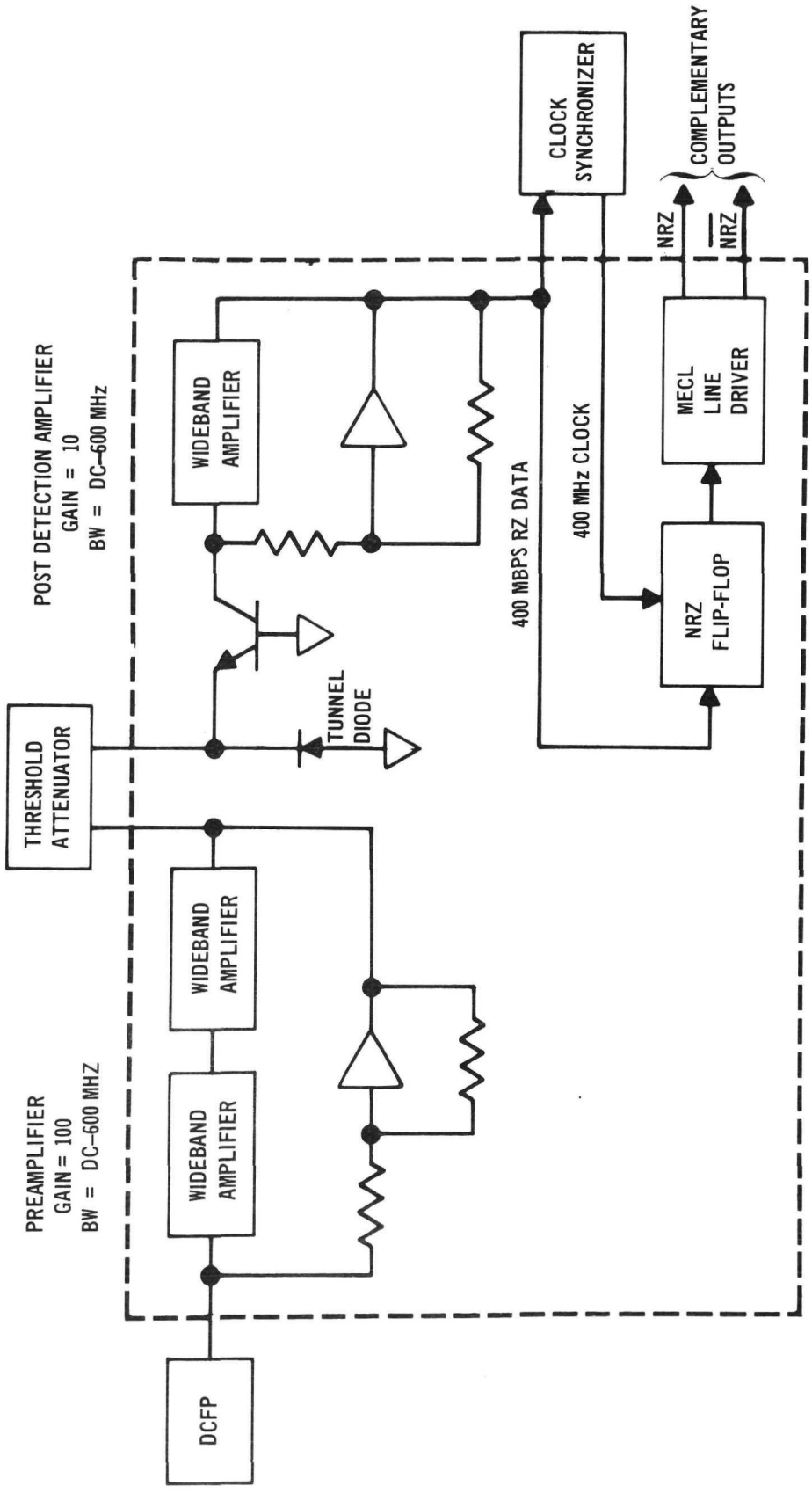


FIGURE 12 THRESHOLD DETECTOR FUNCTIONAL DIAGRAM

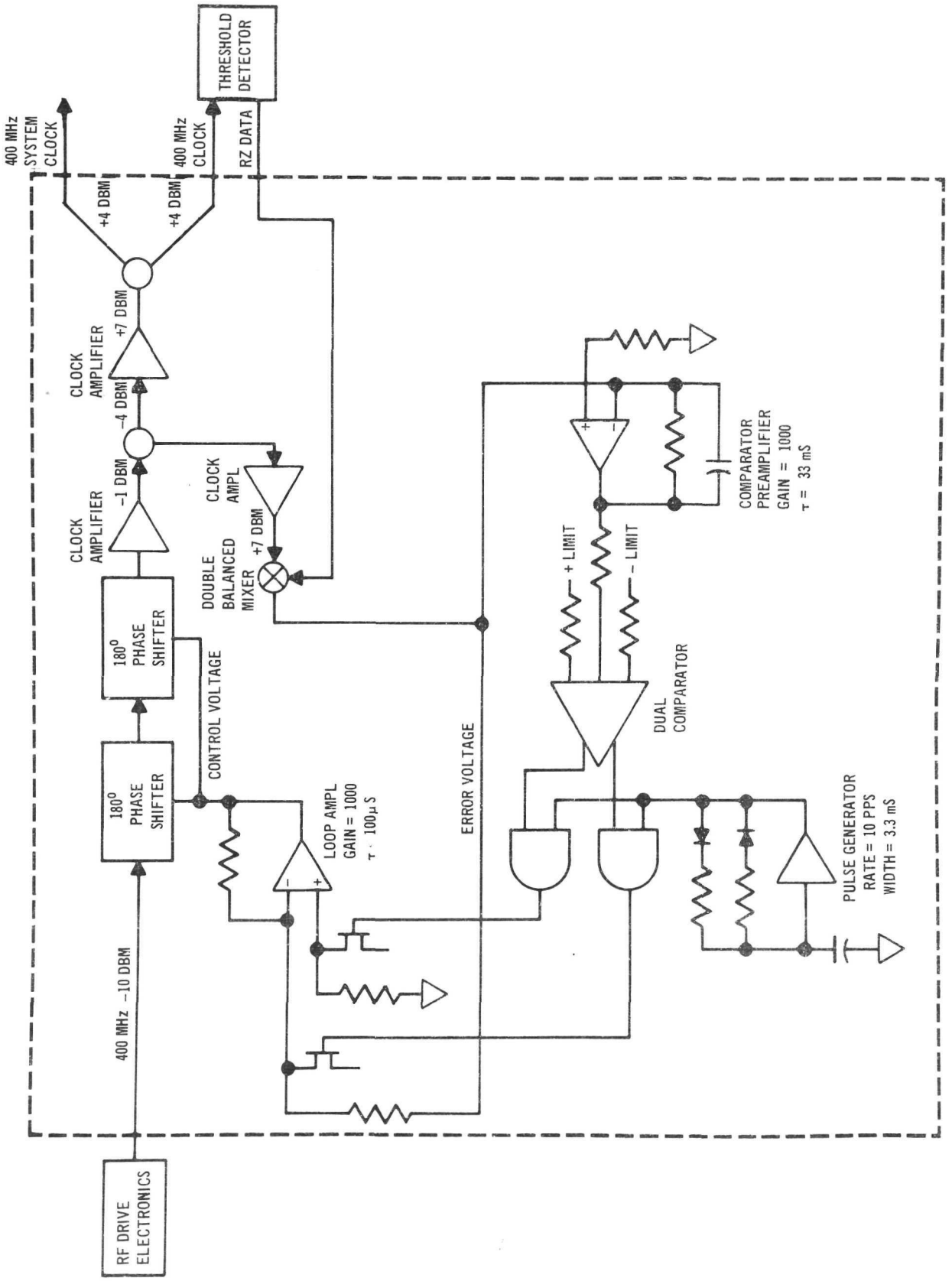


FIGURE 13 CLOCK SYNCHRONIZER FUNCTIONAL DIAGRAM

A second order phase control loop is used to minimize these phase variations. A sample of the RZ data from the threshold detector is taken as a reference and the 400 MHz clock signal from the RF drive electronics is phase shifted to minimize the relative phase error. Two electronic phase shifters are cascaded to give a total control range in excess of 360°. The clock amplifiers and hybrid power splitters provide gain and signal distribution for the synchronized clock signal and a high level drive to the double balanced mixer which acts as the phase error detector in the control loop. The resulting error voltage from the mixer is amplified to produce an approximate closed loop gain of 60.

The remainder of the clock synchronizer electronics is required to make the phase control loop operate modulo 2π. When the phase shifter reaches a phase extreme, the loop saturates and further correction is not possible. The presence of a saturated control loop is detected by the comparator, which gates a pulse from the pulse generator into the loop amplifier. This pulse, when steered to the correct input, forces the loop amplifier to the opposite saturation state thus subtracting 360° from the accumulated phase. After the pulse is removed, the loop corrects toward the linear region of operation since the polarity of the error voltage remains unchanged.

3.7 ERROR RATE ELECTRONICS.

The error rate electronics serially compare a received code with a similar internally generated code. The occurrence of a discrepancy between the codes generates an error signal. The error signals are counted in a fixed time interval to determine error rates.

The error rate electronics automatically synchronize the internally generated code to the received code. A block diagram of the error rate electronics is shown in Figure 14.

The 400 Mbps pseudo-random (PN) code pulse train is amplified by Buffer Amplifier number 1. One of the outputs is routed thru a coaxial delay line (D3), which is changed to correspond to the various PN code lengths available. This system has been designed to operate with code lengths of

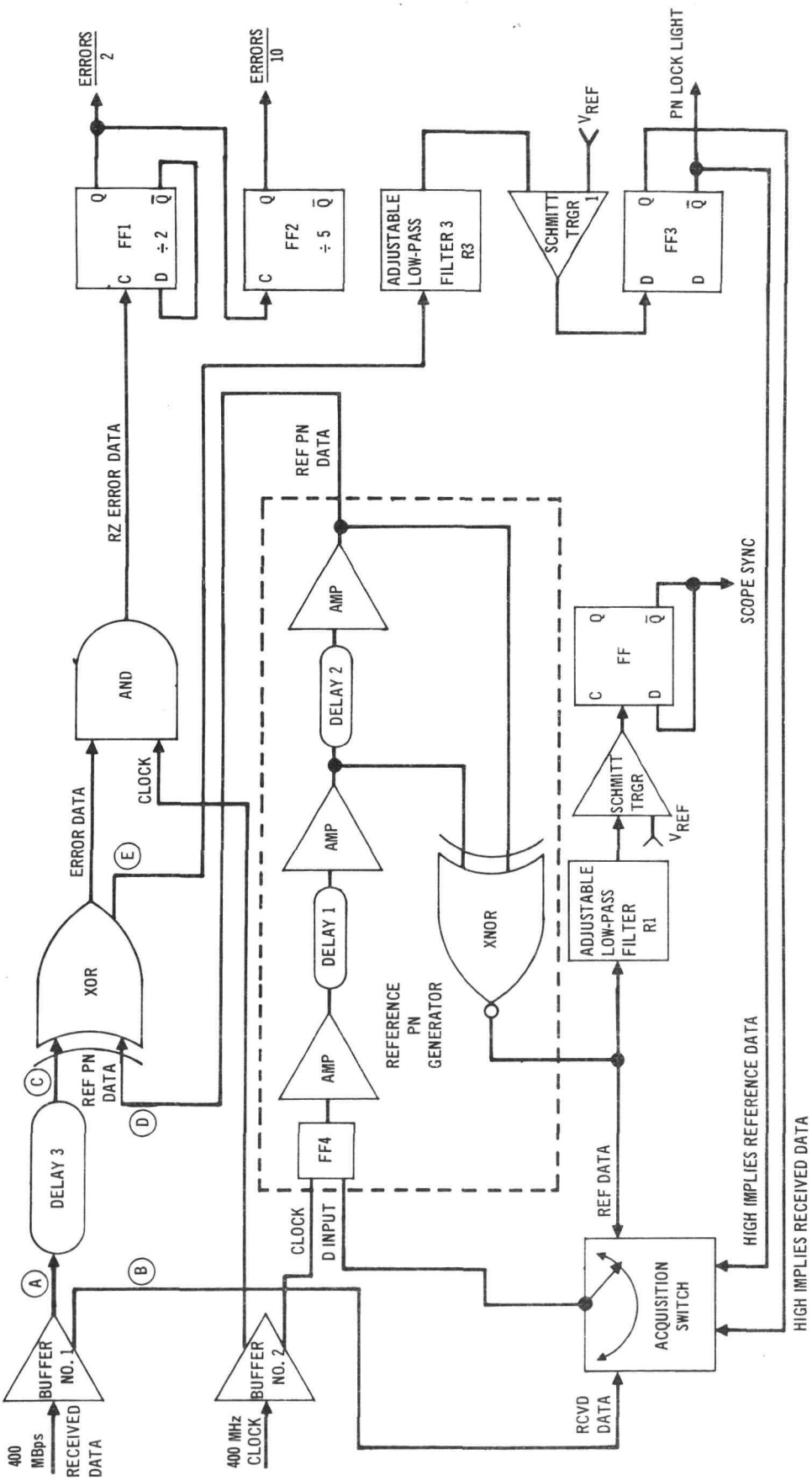


FIGURE 14 ERROR RATE ELECTRONICS FUNCTIONAL DIAGRAM

6, 7, 9, 10, 11, and 15 stages. The PN code, after having been delayed, is used as one input to the exclusive OR (XOR) gate. The other input to the XOR gate is the reference PN code, which is generated by the reference PN generator within the error rate electronics.

The reference PN generator delay cables (D1 & D2) should be selected to generate a reference PN code which is the same stage length as the code being received.

The two PN codes are compared in the XOR gate, and if the two codes are alike in every bit, there is a constant low level out of the XOR. One of the outputs of the XOR is an input to the AND gate, where a logical AND is performed with a 400 MHz clock signal which is synchronized with the PN codes. The AND gate output is routed to a flip-flop where the AND output frequency is divided by two. This signal is available on an external jack (Errors/2) for input to a frequency counter of 50Ω input impedance. This signal is also connected to FF2 where the frequency is divided by five, and this output is also available on a jack (Errors/10).

The XOR gate output is high each time the PN code inputs disagree. The AND gate output is high each time the PN codes disagree and the clock is high The Errors/2 output is high once for each two input pulses to FF1 and the Errors/10 output is high once for each ten input pulses to FF1, or five input pulses to FF2.

The second output of Buffer Amplifier 1 is used as one of the inputs to the acquisition switch. The second input to the acquisition switch is the reference PN code. The output of the acquisition switch is either the received PN code, or the reference PN code, depending on the position of the switch. If the received and reference PN codes agree, i.e. the XOR gate output is low, the acquisition switch will be in the reference PN code position. If the reference PN generator loses synchronization with the received PN code, the output of the XOR gate will be high for considerable lengths of time. This condition will be detected by lowpass filter number 3, and Schmitt trigger number 1. The output of the Schmitt trigger will go high, and cause the Q output of FF3 to become high. This condition causes the acquisition switch to switch to the received PN code position.

With the acquisition switch in the received PN code position, the received PN code is the output of the switch, and the input to the reference PN generator. The reference PN generator then acquires the received PN code, and again becomes synchronized to the received code. Shortly after synchronization is obtained, the XOR gate output goes low, the Schmitt trigger output and the Q output of FF3 become low, $\bar{Q}$ of FF3 becomes high, and the acquisition switch switches to the reference PN code position once again.

Low-pass filter number 3 can be adjusted, in most instances, to distinguish between a large number of errors in the received PN code, and loss of synchronization; however, if the received signal is either a constant high, or constant low, the XOR output appears similar to the loss of synchronization condition. This is of little consequence, since the reference PN generator does not re-establish synchronization until a satisfactory PN code is received.

The synchronization light is illuminated while the reference PN generator is synchronized with the received PN code, and is extinguished when synchronization is lost. Error counts should be ignored during the time the synchronization light is off.

3.8 POWER AND CONTROL UNIT.

The power and control unit operates from a standard 115 Vac, 60 Hz power line and provides low voltage dc power to the receiver electronics, dynode bias to the DCFP, and control and display functions. The three voltages used by the receiver electronics are +15V, -15V and +28V. Primary dc power is obtained from commercial ac/dc power supplies. The secondary dc power requirements include +22V, -5.2V and high voltage dynode bias. The +22V is derived from the 28V supply using a regulator, and the -5.2V is similarly derived from the -15V supply. The dynode bias is produced by two dc-dc inverters. The first dynode inverter is a low current device whose output dc voltage is variable from -300V to -450V by controlling the input dc voltage. The second dynode supply is a moderate current inverter which operates from 28V and is controlled from an external potentiometer. A current limiter is included in this supply to set the maximum available current at 1 mA. Both dynode inverter outputs require

filtering to reduce ripple frequency components. The control and display functions available on the front panel are shown in Figure 2. The power on switch controls ac power to the ac/dc supplies. The power indicator lamp is connected to the 28V supply. The gain control mode is selectable between manual and AGC. In the manual mode the potentiometer controls the gain while in the AGC mode the gain is adjusted by the AGC control loop. In both cases the second dynode current is displayed on the 1 ma full scale meter.

The remaining switch selects the synchronization mode to be used. In the INT position the receiver electronics acquire synchronization while in the EXT position power is removed from certain of the synchronization circuits and an external clock must be supplied to the receiver. The sync loop lock indicator lamp is illuminated when synchronization is acquired in the INT sync mode.

4. OPERATING INSTRUCTIONS

These precedures contain instructions for using the 400 Mbps receiver, indicating configuration definition for various operating modes, adjustment of various receiver operating parameters, specification of receiver interfaces and some measurement methods for evaluating receiver performance.

4.1 INITIAL INSTALLATION.

The receiver mounting plate should be secured firmly to the optical table to insure mechanical stability. The control electronics power cable should be connected to the power and control unit, and 117 Vac 60 Hz applied to the ac power connector.

4.2 INPUT BEAM.

4.2.1 Beam Positioning. An optical method for adjusting the beam should be provided to allow for both vertical and horizontal displacement on the DCFP photocathode.

4.2.2 Beam Size. The beam size at the photocathode should be as small as practical. Typical spot sizes used for testing the receiver are 0.20 mm - 0.25 mm diameter.

4.2.3 Beam Intensity. The receiver is designed to work with optical signal levels corresponding to 30 photoelectrons/pulse to 1000 photoelectrons/pulse. At a quantum efficiency of 4% this corresponds to optical powers of 55 nW- 1900 nW for a data rate of 400 Mbps (50% duty cycle). The absolute maximum optical power should not exceed 3.0 microwatts.

4.3 DCFP OPERATING PARAMETERS.

4.3.1 Dynode Voltage Adjustments. The static component of the electric field is provided by two independently adjustable high voltage supplies, one for each dynode. The two dynode biasing fields are designated E01 (dynode 1) and E02 (dynode 2). The adjustments for E01 and E02 are on the rear of the power and control unit. Also included are test jacks for monitoring the two

dynode voltages. Caution should be used in measuring these voltages as they are typically -400 Vdc and a floating voltmeter must be used. E01 should be set at -410 Vdc and left at this value. The setting of E02 is dependent upon the desired receiver characteristics. For maximum DCFP gain the recommended value for E02 = -365 Vdc.

The next operating point is for one less gain step and occurs at E02 = -400 Vdc. The third operating point occurs for E02 = -465 Vdc, and this point sacrifices DCFP gain but yields better electron bunching, higher collector efficiency, and a somewhat better system error rate.

4.3.2 Magnetic Field Adjustments. The magnetic field should not require adjustment under normal receiver operation. However an adjustable screw is provided on each side of the detector head which allows the field to be varied. The number of turns from the full in position are calibrated in gauss as indicated in the calibration chart below. The normal setting is underlined.

TABLE 2

MAGNETIC FIELD CALIBRATION FOR DCFP S/N013.

TURNS FROM FULL IN POSITION (Both Screws)	MAGNETIC FIELD GAUSS
0	330
1/2	335
1	345
1 1/2	350
2	370
2 1/2	380
3	390
4	400
5	410

4.3.3 RF Interlock. The DCFP is provided with an interlock feature that prevents RF drive power from being applied unless both dynode voltages are adequate to prevent damage to the DCFP. The small circuit board within the mount provides this function. Switch S1 on this board allows for disconnecting the voltage sensing element from the first dynode. This should only be done when DCFP photocathode current is being measured. The "up" position for switch S1 is the photocurrent mode, and the "down" position is the normal operating position.

4.4 SYNCHRONIZATION MODES.

4.4.1 Internal (Remote) Synchronization. In this mode the receiver acquires synchronization from the input optical pulse train. The SYNC MODE switch on the control panel should be in the INT position and jumper cable P13-14 should be in place on the RF drive electronics. When the receiver is phase locked to the optical signal, the sync loop lock indicator will be illuminated.

4.4.2 External Synchronization. The use of an external signal which is phase coherent with the optical pulses may be used to operate the receiver. This is accomplished by applying a 400 MHz signal to the manual phase shifter supplied with the receiver. The required level into the phase shifter is -7 dBm(0.28 Vp-p) $\pm$ 1 dB. The output of the phase shifter is connected to J14 on the RF drive electronics in place of the jumper cable P13-14. The SYNC MODE switch should be in the EXT position for this mode of operation. The phase shifter is adjusted to center the DCFP gate on the optical pulse. This can be observed by monitoring the DCFP output with a sampling oscilloscope. If an NRZ data output is desired when operating in the EXT SYNC mode, an additional synchronous 400 MHz signal must be applied to the Clock Synchronizer input at J16. The level of this signal should be -10 dBm (0.20 Vp-p) $\pm$ 1 dB and requires no external phase shifter.

4.5 GAIN CONTROL MODES.

4.5.1 Automatic Gain Control (AGC). The AGC mode is considered to be the normal operating mode for the detector. This mode is implemented by the DCFP gain switch being set to the AUTO position. When operating in the AGC mode, the optical signal may be varied without re-adjusting other receiver parameters. The meter on the control panel measures the DCFP second dynode current. Full scale for this meter is 1.0 mA. When operating in the AUTO mode, the AGC maintains the second dynode current constant at 0.3 mA over the receiver dynamic range. This value of 0.3 mA is a trade-off between required tube gain and pulse output amplitude. This value can be changed to any value from 0.15 mA to 0.50 mA by adjusting pot R45 on the Sync Loop Electronics Board 1. Since the AGC loop senses the average second dynode current, any long term change in data duty cycle will change the output pulse height correspondingly. This is normal.

4.5.2 Manual Gain Control. A manual gain control mode is also provided whereby the DCFP gain is varied by the MANUAL GAIN knob on the control panel. Before switching the DCFP gain switch to the MAN position the MANUAL GAIN control should be set to the extreme clockwise limit (minimum gain). Again the operating second dynode current is measured by the panel meter. An upper limit of 0.5 mA is recommended for long DCFP life. If the current exceeds 0.7 mA the current limiter in the second dynode power supply begins to reduce the bias voltage. A point is reached where the interaction of the current limiter and RF interlock results in an audible relay chatter in the power and control unit. This condition should not be allowed to remain for any period of time, as it represents an overload condition.

4.6 THRESHOLD DETECTOR.

4.6.1 Preamplifier Input Level. The data preamplifier in the Threshold Detector provides the necessary gain for the DCFP output levels to the tunnel diode operating levels. It is essential that this amplifier be operated in its linear region, so the input level must be attenuated to the extent that the preamp output level at J22 is approximately 400 mV peak-to-peak. The DCFP output pulse amplitude will vary depending on the number of gain steps

selected by varying E02, the dynode current, and the duty cycle of the digital data. A 6 dB broadband resistive signal splitter provided at the DCFP output serves as an attenuator and as a signal monitor test point. An additional 3 dB or 6 dB pad in the input line should be used if the level at J20 exceeds 400 mV.

4.6.2 Threshold Attenuator Setting. The variable attenuator on the receiver mounting plate provides the means of adjusting the amplitude of the pulse going to the tunnel diode threshold detector. The optimum setting for this attenuator is dependent on optical signal power and preamplifier output level. To set it properly the NRZ data output should be monitored at J25 either with error rate instrumentation or a sampling oscilloscope. The former method is much more sensitive and is therefore preferred.

4.7 RECEIVER OUTPUTS.

4.7.1 NRZ Data Output. Complimentary NRZ data outputs are provided at J25 and J26. The levels are standard MECL levels of -800 mV and -1600 mV.

4.7.2 Synchronous Clock Output. A 400 MHz clock is available at J19. This clock is always synchronous with and maintains the same phase relationship with the NRZ data. The amplitude of this clock is nominally +4 dBm into a 50 ohm load.

4.7.3 200 MHz Clock. A 0 dBm 200 MHz clock is available at J15 of the drive electronics when operating in the internal synchronization mode.

4.8 DCFP PHOTOCURRENT QUANTUM EFFICIENCY MEASUREMENT.

To measure the DCFP photocathode current, observe the following procedure:

(1) Turn off power to the receiver
(2) Disconnect P1 from J1
(3) Remove DCFP enclosure cover. Move interlock switch S1 in the DCFP enclosure to the UP position.
(4) Place magnetic field shorting plate into position inside the DCFP assembly.

(5) Connect a 300 volt battery and nanoammeter to P1 as shown in Figure 15 .

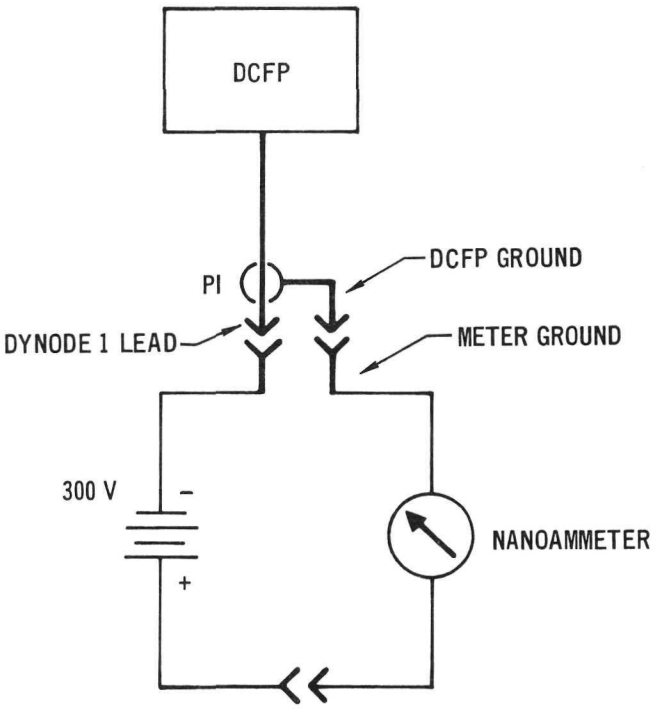


FIGURE 15 SETUP FOR PHOTOCATHODE CURRENT MEASUREMENT

(6) Reduce ambient light as much as possible.

(7) Measure the cathode current with and without presence of the 0.53 μm optical beam. The difference is the photocurrent.

(8) Measure the incident power of the optical beam.

(9) Compute photocathode yield = $\frac{\text{photocurrent}}{\text{optical power}}$ in amps/watt.

Multiply by $\frac{100\%}{0.43 \frac{\text{amps}}{\text{watts}}}$ to obtain the quantum efficiency in percent.

4.9 ERROR RATE ELECTRONICS.

A Reference PN Generator within the Error Rate Electronics is automatically synchronized to the incoming data stream, and a PN lock light is illuminated when the received and reference PN codes are phase aligned. The two PN codes are compared serially to obtain the error count. This count is divided by two and divided by ten. The "errors divided by two" signal is available on J17, and the "errors divided by ten" signal is available on J19. These signals should be monitored with a frequency counter which has a 50 ohm input impedance. A scope synchronization signal is available on J21. (50 ohms)

The supply voltage required is -5.2 volts dc, and the power supply used should be capable of supplying at least two amperes. Power dissipation is approximately 10 watts total.

The received PN code must be synchronized with the 400 MHz clock signal, and the received PN code should be approximately the same shape as the reference PN code. Input and output signals are specified below:

Inputs: 1. Received PN data stream:
400 Mbps, NRZ, pseudorandom noise code. MECL level, DC coupled. Error rates can be measured on codes of 6, 7, 9, 10, 11, and 15 stages.
The rise and fall times of the received pulses should be approximately 1.5 nanoseconds (10% to 90%).

2. Clock:
400 MHz sinusoidal waveform, 1 volt peak-to-peak, ± 5 volts maximum dc offset, synchronized to incoming data.

Outputs: Scope Synchronization Trigger and Error Outputs:
900 mV, peak-to-peak, biased about -2.1 volts dc.

All cables should be connected as numbered, with the number on the end of the cable corresponding to the J number on the jack. Delay cables numbers 1, 2, and 3 should be selected to correspond to the stage length of the code being received. These cables are labeled according to code length, cable number, and cable length. All the cables, with the exception of the error outputs and the scope sync cables, are cut to specific lengths. These lengths are necessary to insure that all signals are correctly aligned. The correct cable lengths are also listed in Table 3.

Once power is applied, connect all cables with the exception of J10 and J16. Monitor J15 with an oscilloscope. The 400 Mbps NRZ reference PN code should be present. The synchronization light should be illuminated since there are no inputs to the XOR gate. Next, monitor J21 and adjust R1 for a square wave with a half period as indicated in Table 4. This period is determined by the stage length of the PN code.

Connect a cable from J21 to the external synchronization trigger input on the oscilloscope. The signals can all be monitored using J21 as the external sync. Since the scope sync signal is derived from the reference PN generator the signal will be erratic during periods when the received and reference PN codes are not synchronized.

Connect the proper cables to J10 and J16, and connect J17 or J19 to a frequency counter with 50 ohms input impedance. If J17 is used, the count should be multiplied by two to obtain the actual error count, and if J19 is used, the count should be multiplied by ten. The error counts should be recorded only when the synchronization light (DS1) is illuminated. When this light is extinguished, the reference PN generator is no longer synchronized with the received PN code.

When there is no data present on J16, the synchronization light will be illuminated, but is will not be as bright as when synchronization is obtained. During this condition, the acquisition switch will be switching back and

TABLE 3

ERROR RATE ELECTRONICS CABLE LENGTHS

CABLE DESIGNATION	PSEUDORANDOM CODE STAGE LENGTH 6	7	9	10	11	15
D1	22*	43	26	62	103	198
D2	2	2	59	42	20	4.5
D3	96	119	156	175	196	276
Clock Input	121.25 →					
Data Input	51.5 →					
P3-4	3.5 →					
P5-6	3.5 →					
P7-8	3.5 →					
P9-10	3.5 →					

* All Cable Lengths in Inches.

TABLE 4

PSEUDORANDOM CODE SEQUENCE DURATION

PSEUDORANDOM CODE STAGE LENGTH	SEQUENCE DURATION*
6	157.5 ns
7	317.5 ns
9	1277.5 ns
10	2557.5 ns
11	5117.5 ns
15	81917.5 ns

* Scope Sync period equals twice sequence duration

forth between the reference PN generator and the received data line. Since there is no data present on the received data line, the output of the XOR gate will consist of approximately one sequence length of PN data followed by a low signal of approximately the same length. This total signal has a higher dc value than when synchronization is obtained, but not as high as the unsynchronized condition when data is present on J16. As a result, the synchronization light will be of intermediate brightness.

The following test can be run if difficulties are encountered during error rate measurements. With received data present on J16, adjust R3 until the synchronization light is competely extinguished. The error count should then be very low, usually zero, unless the received data has an extremely high error rate. The XOR operation is being performed between the received data, and the same received data after propagation thru the reference PN generator. This test checks the length of the data cables D1, D2, and D3. To readjust the low-pass filter, remove J16 and adjust R3 until the synchronization light is illuminated. Then rotate R3 in the opposite direction until the light begins to extinguish. Reconnect J16.

5. PERFORMANCE TESTS

This section discusses the performance tests applied to the gated high speed optical detector and the error rate electronics.

5.1 GAIN CHARACTERISTICS.

The DCFP was operated in a special test set up in which fixed operating biases were maintained at preset levels. The RF drive was derived directly from the laser transmitter output rather than using the remote synchronization circuitry. Input photocathode current in response to the laser transmitter signal was calibrated against a precision variable optical attenuator placed in the optical beam. Anode output current was then plotted versus input current at various RF drive power levels. The dc dynode bias was adjusted slightly to compensate for step size variations with RF drive level. The resultant transfer characteristics for DCFP S/N013 are presented in Figure 16. The number of steps in each case is the same, except that an error in bias voltage resulted in one less step for the 0.5 watt curve. The linearity of these curves is excellent up to 0.5 mA of second dynode current.

5.2 QUANTUM EFFICIENCY.

The photocathode quantum efficiency of each DCFP was determined by measuring the photocurrent due to a known optical signal level. DCFP photocurrent was measured by operating the DCFP as a photodiode, with magnetic field and RF drive power removed. With only the dc electric field bias acting on the photoelectrons, they were accelerated to and collected by the rail electrode which was at ground potential. The cathode response in amps per watt was compared with the theoretical maximum of one electron per photon, which was 0.43 amps per watt at 0.53 μm and 0.86 amps per watt at 1.06 μm, in order to determine the quantum efficiency.

The quantum efficiency of DCFP S/N 013 at 0.53 μm averaged 3.7% over the entire cathode and had two hot spots of 4.0% and 5.0%.

The quantum efficiency of DCFP S/N013 at 1.06 μm was 0.005%.

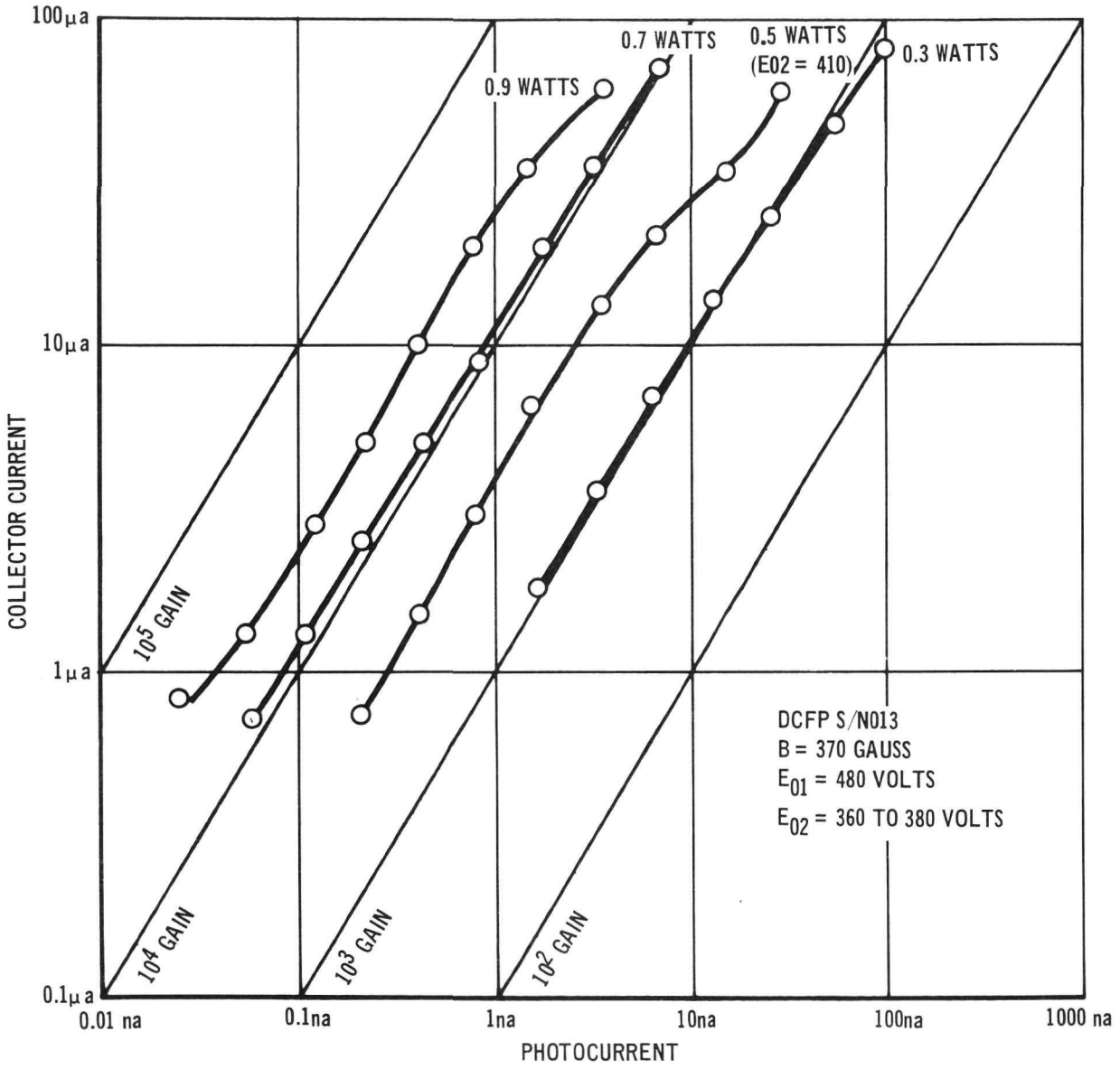


FIGURE 16 DCFP S/N 013 CURRENT GAIN

5.3 COLLECTOR EFFICIENCY.

The collector efficiency is the portion of the second dynode current which is delivered to the anode and is a function of the DCFP operating conditions. At lower gain and fewer multiplication steps, the phase focusing and bunching is tighter, and a greater fraction of the dynode current passes through the collector aperture to reach the anode. The chosen operating conditions for DCFP S/N 013 in the 0.53 μm detector head (E02 = -465 volts) result in a collector efficiency greater than 20% over the operating range.

5.4 GATING.

Gating is measured by a convolution technique in which the narrow mode locked laser pulses are used to sample the shape of the DCFP gating function. The DCFP gating function is synchronous with the RF drive. The RF drive frequency is chosen to be slightly different than the frequency of the incoming optical pulse train. Each succeeding pulse is then received at a different portion of the DCFP gating function which in turn affects output pulse amplitudes corresponding to the degree of gating. The envelope of the output pulse train then reproduces the shape of the gating function at the difference frequency to an accuracy limited by the laser pulse width. If the DCFP output is displayed on a low frequency oscilloscope, integration of this output pulse train results in a display of the envelope which is the convolution of the optical pulse train with the DCFP gating function.

The convolution waveforms of DCFP S/N013 with normal and optimal operating biases are shown in Figure 17 in response to a 400 Mpps mode locked laser pulse train.

5.5 ACQUISITION AND SYNCHRONIZATION.

Testing of the acquisition and synchronization functions was designed to measure the static and dynamic limits of loop performance.

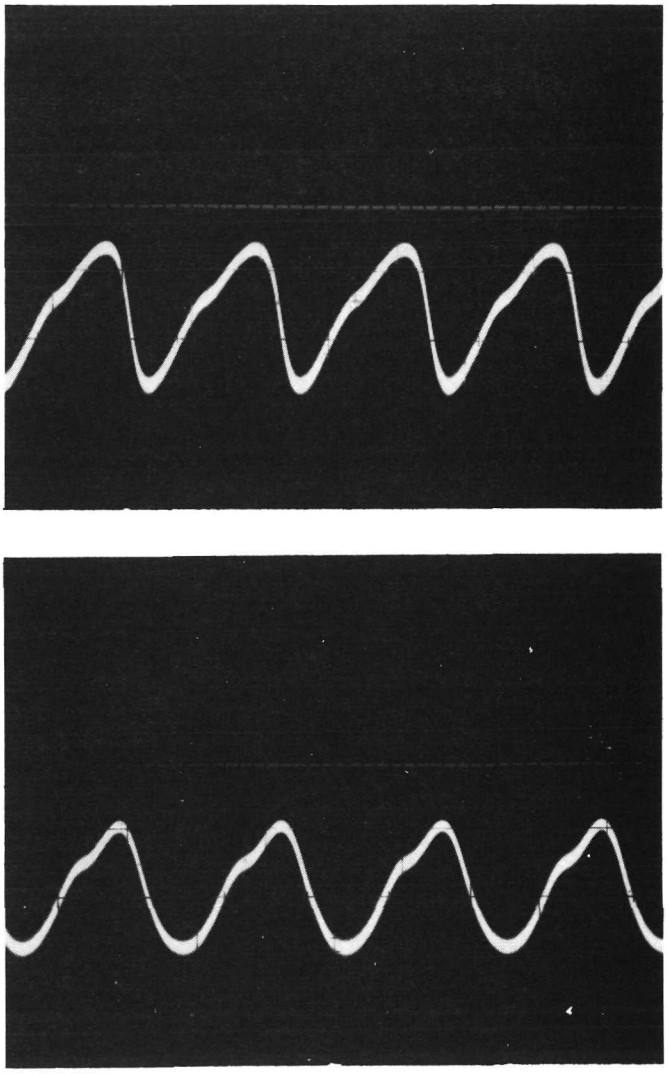


FIGURE 17 CONVOLUTION OF DCFP S/N013 GATING FUNCTION

To measure the static acquisition range, the frequency of the 400 Mpps mode locked laser was offset a fixed amount and the optical signal power level reduced until acquisition threshold was reached. The results of this test are shown in Figure **18**.

The dynamic performance of the synchronization loop is described by the deviation-rate product. This figure was measured by frequency modulating the test laser with a triangular modulating waveform at a peak deviation of ± 1.7 kHz and slowly increasing the modulation frequency until the loop lost lock. With a large input signal, the laser pulse repetition frequency was modulated with 3.3 kHz peak to peak deviation 480 times per second before the acquisition circuitry was unable to track the incoming signal. Therefore, the allowed

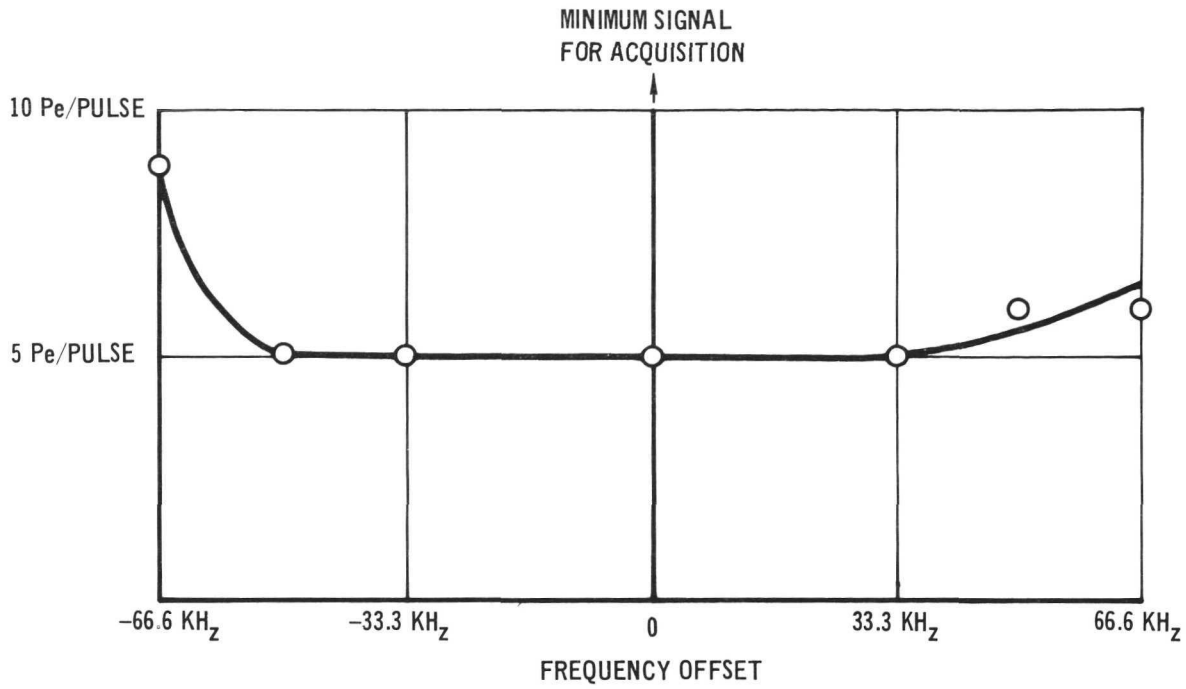


FIGURE 18 STATIC ACQUISITION RANGE

transmitter deviation rate product is 1.6×10^6 Hz/sec. It is estimated that this figure is greater than $3 \cdot 10^5$ Hz/sec for input signals down to 30 photoelectrons per pulse.

The loop bandwidth and damping factor were estimated at 1 kHz and 0.7 respectively using a similar test at lower deviation with a sinusoidal modulating signal.

5.6 RF DRIVE CHAIN.

The spectral purity of the RF drive chain outputs at 200 MHz, 400 MHz and 1200 MHz is shown in Figure 19. The 1200 MHz drive to the DCFP is variable over a range of 0.1 to 1.9 watts.

5.7 AUTOMATIC GAIN CONTROL.

The characteristics of the dynode AGC loop were specified by static error of the dynode current and illustrated by photographs of the output pulse amplitude of the DCFP detector.

The static error was a measure of the change in dynode current as the optical input signal was varied over the specified dynamic range. The results

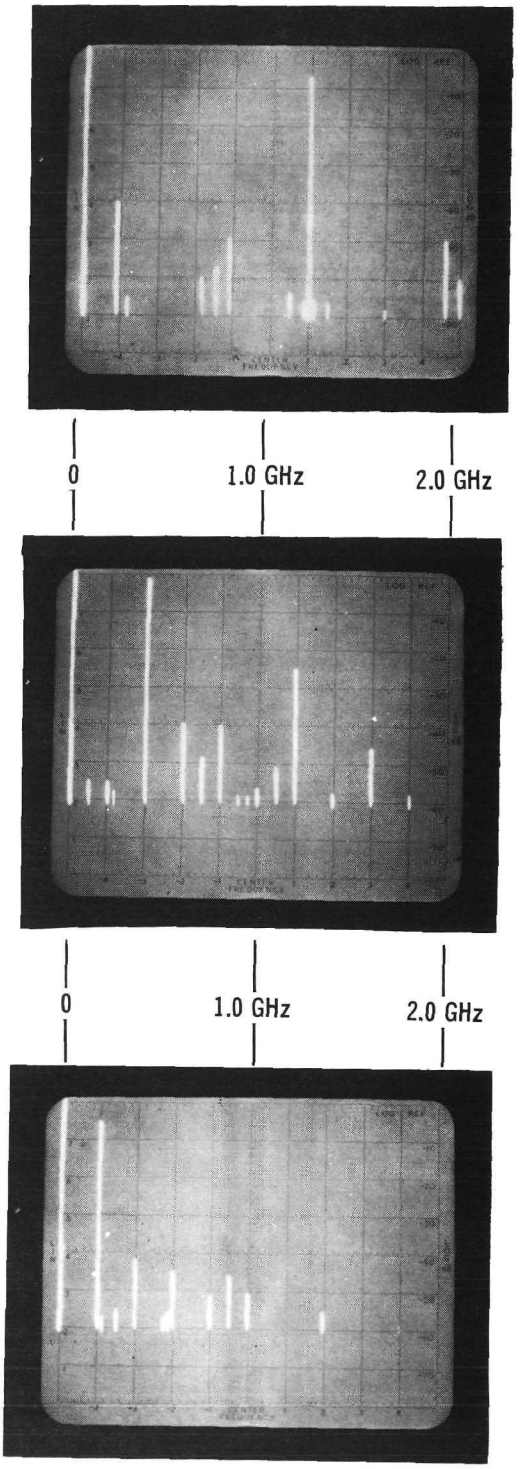


FIGURE 19 RF DRIVE ELECTRONICS OUTPUTS

of this test are presented in Table 5. The closed loop frequency response of the AGC loop was measured to be 10 kHz at -3 dB down. The estimated tracking response of the dynode 2 bias compensator is 30 Hz.

The effect of AGC and E02 bias compensation on the detector output pulse is shown in Figure 20. These photographs demonstrate that the receiver had a dynamic range of input optical power greater than 15 dB (corresponding to a 30 dB range of detected photocurrent). The different E02 voltages indicate the amount of bias compensation required to change step size to keep the output pulse centered in the dynode collector aperture.

5.8 THRESHOLD DETECTOR.

Following is a summary of measured characteristics of the Threshold Detector:

Preamplifier Bandwidth	dc - 600 MHz $\pm$ 1.5 dB
Preamplifier Gain	100
RZ Input Range	10 - 20 mV peak
Threshold Resolution	1 dB
Post Detection Amplifier Bandwidth	dc - 700 MHz $\pm$ 1.5 dB
Post Detection Amplifier Gain	10
NRZ Output Levels	-800 mV and -1600 mV

Threshold resolution is a measure of the width of the threshold uncertainty region. Resolution is expressed in dB and is defined as 20 $\log_{10} V_1/V_o$ where V_1 is the minimum signal voltage level which always results in a "one" count and V_o is the maximum level which always results in a "zero" count at the threshold detector output.

Figure 21 shows various threshold detector waveforms. Figure 21A shows the preamplifier input and output. Figure 21B shows the output of the tunnel diode threshold detector and post detection amplifier for the same input signal. Figure 21C is the clock/data relationship which was required at the NRZ flip-flop for proper conversion to NRZ format. Figure 21D is the NRZ data output and the output 400 MHz clock.

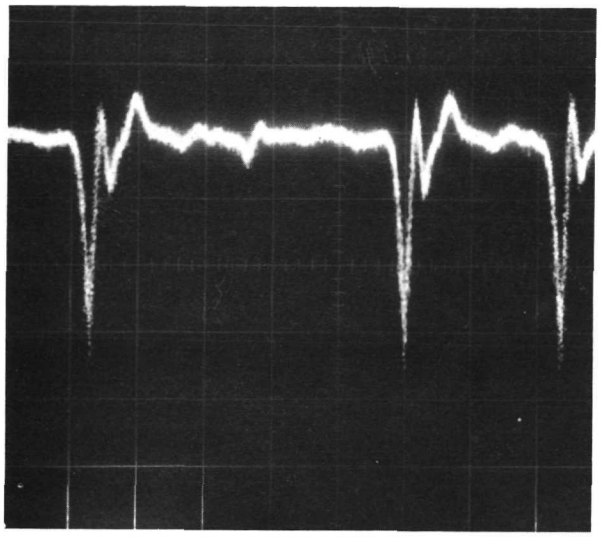
5.9 CLOCK SYNCHRONIZER.

The essential requirement for the clock synchronizer is to keep the clock phase fixed with respect to the data. The second order control loop had the following measured parameters:

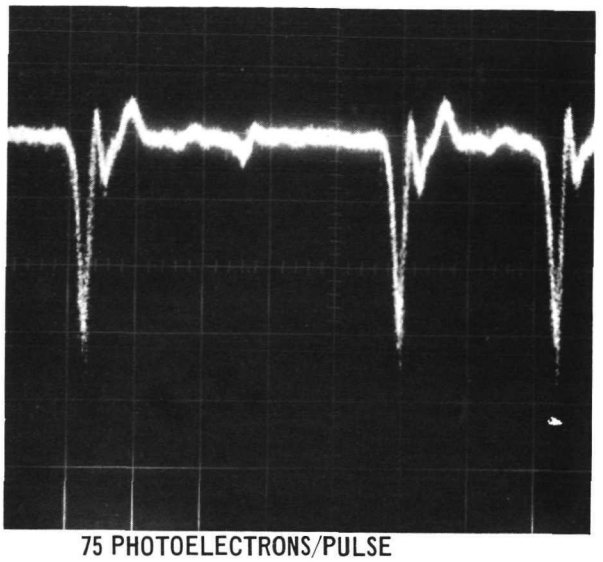
TABLE 5

STATIC AGC CHARACTERISTICS

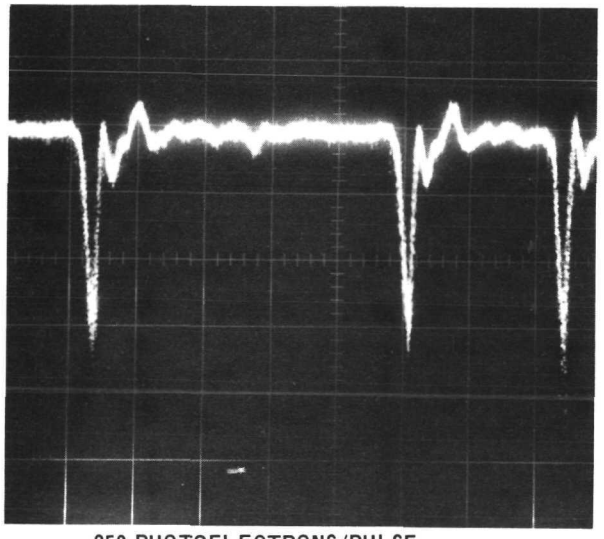
Optical Input Signal Level (pe/pulse)	2nd Dynode Current (μa)	Static Error
25	294	-2.0%
50	296	-1.3%
100	299	-0.3%
200	300	0
300	301	+0.3%
450	302	+0.7%
600	304	+1.3%
750	304	+1.3%



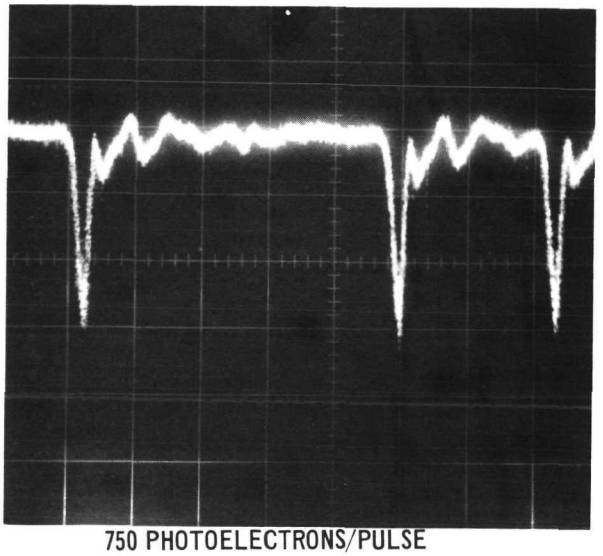
25 PHOTOELECTRONS/PULSE
E_{02} = –357 VOLTS P_{RF} = 0.95 WATTS



75 PHOTOELECTRONS/PULSE
E_{02} = –359 VOLTS P_{RF} = 0.76 WATTS



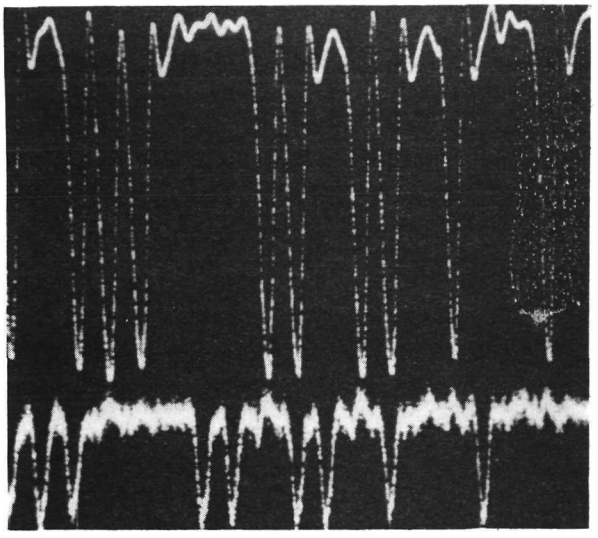
250 PHOTOELECTRONS/PULSE
E_{02} = –361 VOLTS P_{RF} = 0.58 WATTS



750 PHOTOELECTRONS/PULSE
E_{02} = –364 VOLTS P_{RF} = 0.43 WATTS

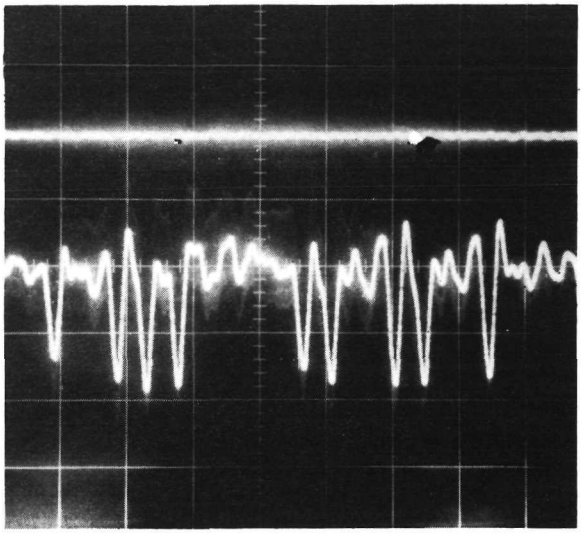
VERTICAL 10 mV/DIV
HORIZONTAL 1 nSEC/DIV
E_{01} = –408 VOLTS
B = 380 GAUSS
Id_2 = 300 μa

FIGURE 20 DCFP S/N013 OUTPUT WITH AGC



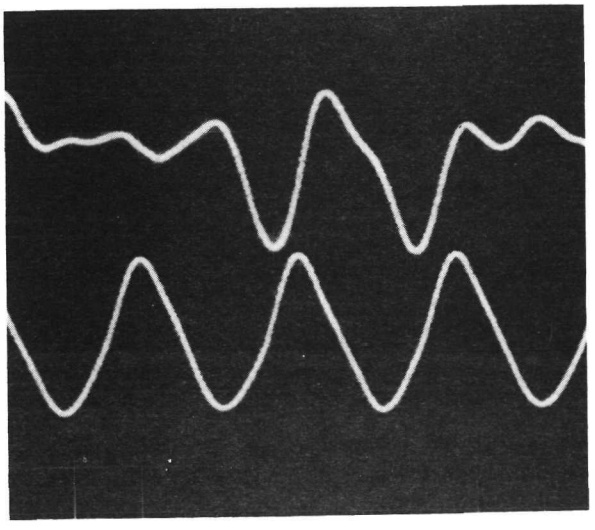
A

(upper) PREAMPLIFIER OUTPUT
(lower) PREAMPLIFIER INPUT
HORIZONTAL 5 nSEC/DIV



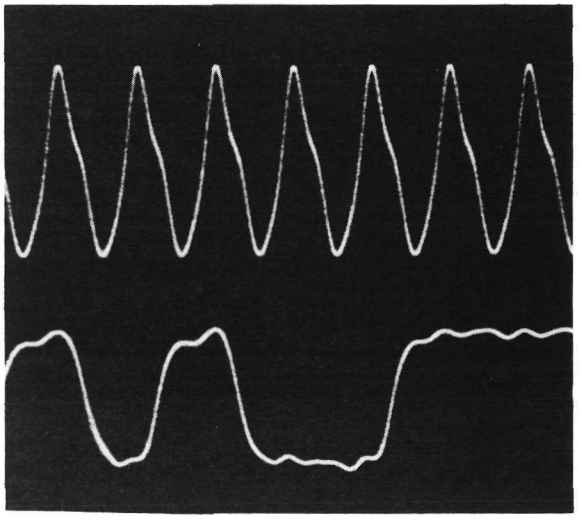
B

POSTAMPLIFIER OUTPUT
400 mV/DIV, 5 nSEC/DIV



C

NRZ FLIP FLOP INPUTS
(upper) RZ DATA
(lower) 400 MHz CLOCK
400 mV/DIV, 1 nSEC/DIV



D

RECEIVER OUTPUTS
(upper) 400 MHz CLOCK
(lower) NRZ DATA
400 mV/DIV, 2 nSEC/DIV

FIGURE 21 400 Mbps – THRESHOLD DETECTOR WAVEFORMS

Closed Loop Gain	65
Closed Loop -3 dB Bandwidth	40 kHz
Static Phase Error	$\pm$ 6° maximum

These closed loop parameters were measured by electronically phase shifting the clock input signal to the clock synchronizer. The bandwidth was measured by phase modulating the clock signal with a variable frequency sine wave. The static phase tracking error is shown in Figure 22 as a function of phase difference between the clock and data signals. The worst case static error of $\pm$ 6° corresponded to a timing error of $\pm$ 42 picoseconds at the input to the NRZ conversion flip-flop. This was well within the requirement of $\pm$ 80 ps for proper flip-flop operation.

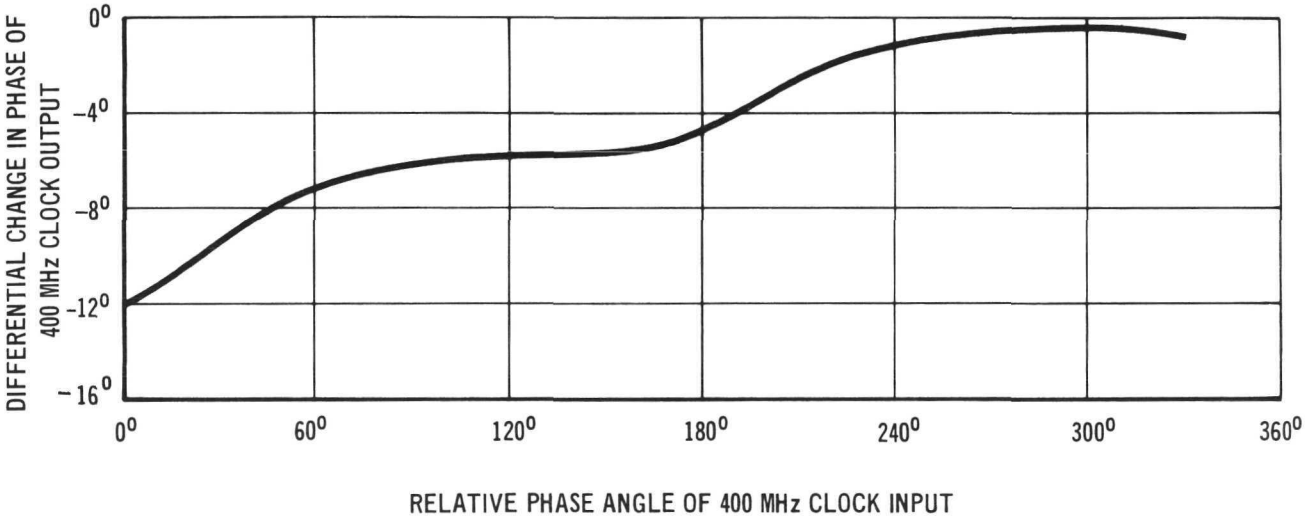
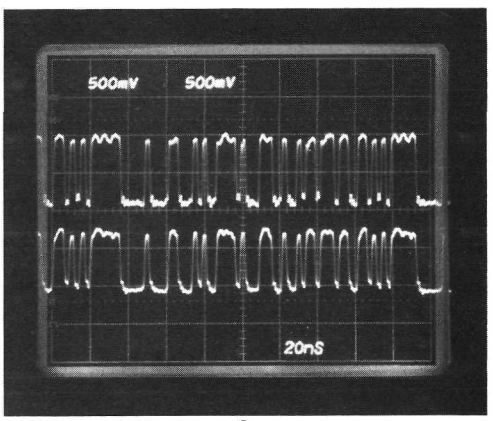


FIGURE 22 STATIC CLOCK SYNCHRONIZER PHASE ERROR

5.10 ERROR RATE ELECTRONICS.

The Error Rate Electronics was operated using a pseudorandom code generator as the input test signal source. These tests were performed with each of the six pseudorandom code sequence lengths. The photographs shown in Figures 23, 24, and 25 were taken using the six stage code. This code is sixty three bits, or 157.5 nanoseconds long.

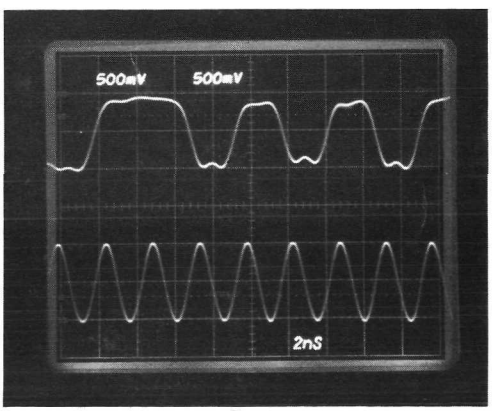
The pseudorandom code input to the Error Rate Electronics is shown in Figure 23A and B. The input clock signal was the 400 MHz sine wave shown in the lower part of Figure 23B. The Reference Pseudorandom Code Generator output is shown in Figure 23A.



A

RECEIVED PN CODE (INPUT)

INTERNAL REFERENCE PN CODE

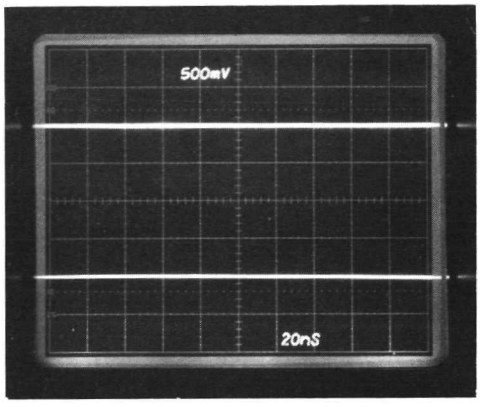


B

RECEIVED PN CODE

400 MHz INPUT CLOCK SIGNAL

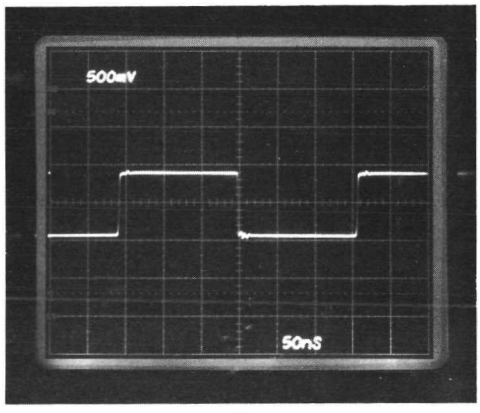
FIGURE 23 ERROR ELECTRONICS I



A

ERRORS DIVIDED -BY-TWO (OUTPUT)

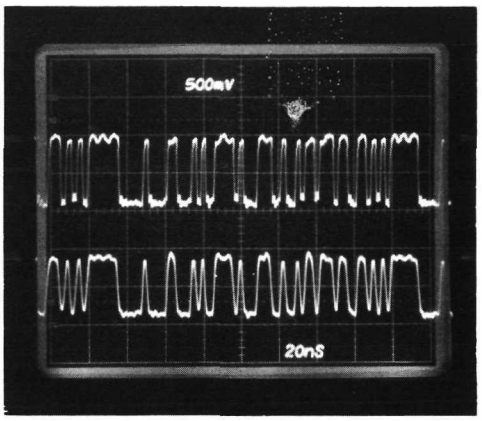
ERRORS DIVIDED-BY-TEN(OUTPUT)



B

SCOPE SYNCHRONIZATION SIGNAL OUTPUT

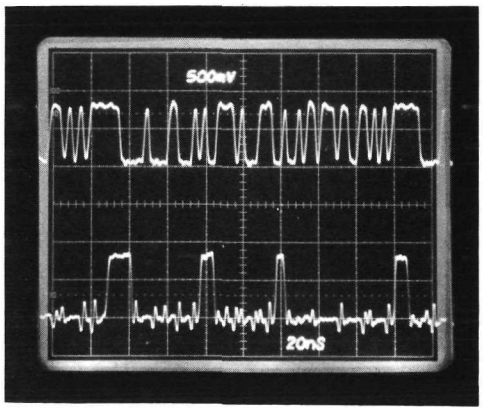
FIGURE 24 ERROR ELECTRONICS II



RECEIVED PN CODE (INPUT)

ERRORS DIVIDED-BY-TWO (OUTPUT)

A



ERRORS DIVIDED-BY-TWO (OUTPUT)

ERRORS DIVIDED-BY-TEN (OUTPUT)

B

FIGURE 25 ERROR ELECTRONICS III

When the received pseudorandom code and the reference code were out of phase the Error Rate Electronics automatically realigned the reference code generator to the phase of the received code. As a result, under normal conditions, no meaningful test could be made to evaluate the ability of the electronics to measure maximum error rates. The tests with maximum error rates were therefore performed with the acquisition switch disabled. Disabling the acquisition switch prevented realignment of the pseudorandom codes.

Figure 24A shows the input code and the errors divided-by-two output with maximum errors. Figure 24B shows the errors divided-by-two and the errors divided-by-ten with the same error rate. A frequency counter was used to monitor the error outputs, and both of the outputs gave the correct count.

Figure 25A shows the two error outputs with the acquisition switch in the normal condition. Again, a frequency counter was used to check the count, and a constant zero count was present at both outputs.

The scope synchronization signal is shown in Figure 25B. This synchronization signal became erratic during phase realignment, but was stable once realignment was accomplished.

The final tests were run using the 400 Mbps receiver as the input to the Error Rate Electronics. The received data input and the 400 MHz clock must be properly aligned in phase; therefore the cables used for these two signals were cut to specific lengths. The receiver error rate tests gave results which were very close to the theoretical results, as indicated in the Performance Tests.

6. COMMUNICATIONS SYSTEM EXPERIMENT

The gated high speed optical detector and the error detection electronics were operated in an experimental 400 Mbps communication system along with a 400 Mpps mode-locked, frequency doubled Nd:YAG laser and the 400 Mbps optical modulator system. A block diagram of the set up for error rate measurements is shown in Figure 26. The electrooptic modulator encoded the transmitted optical beam with a pseudorandom code. The clock signal for the optical modulator system was derived from the laser output pulse train by means of a photodiode detector and a phase locked loop (rather than from the reference oscillator which drives the laser) in order to eliminate the effect of phase shifts which occur between the reference oscillator and the laser output due to laser cavity length detuning. The optical attenuator simulated the optical attenuation experienced over long transmission distances. The NRZ data output and a 400 MHz clock signal from the receiver were fed to the error detection electronics with suitable relative delay. A pseudorandom code generator in the error detection electronics which duplicated the transmitted code was automatically brought into synchronization with the received code. The error detection electronics then compared the codes serially, and the discrepancies which were detected were counted in a preset time interval and printed. The results of a series of such measurements, using the NASA 0.53 μm detector head, are shown in the error rate curves of Figure 27. No special significance is attached to the fact that the longer code sequences produced lower error rates, since the tests were conducted on different days and all system parameters may not have been faithfully duplicated. Error rates below 10^{-7} were difficult to obtain because the test laser amplitude was not sufficiently stable for the extended counting periods required.

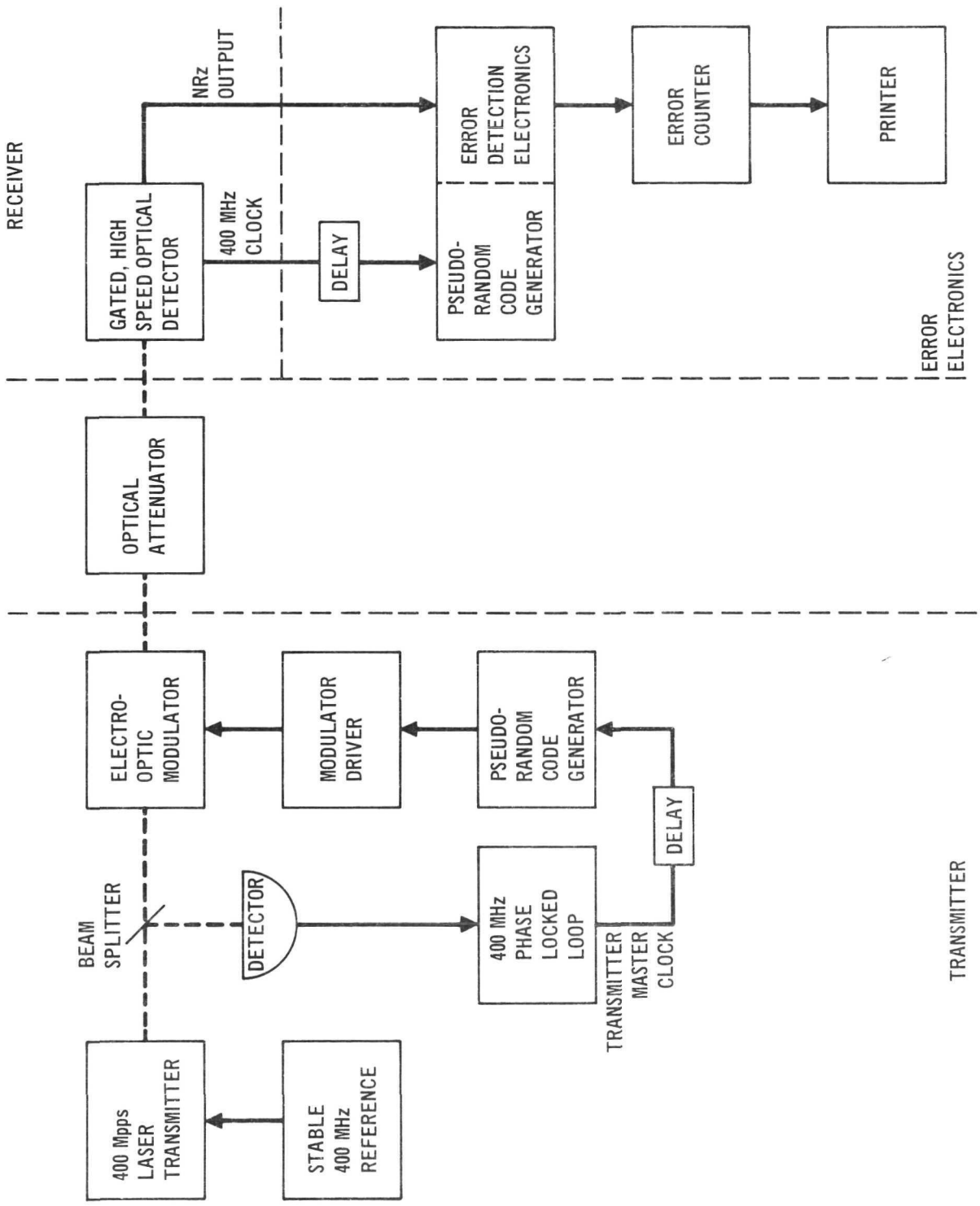


FIGURE 26 EXPERIMENTAL SETUP OF COMMUNICATION SYSTEM ERROR RATE MEASUREMENT

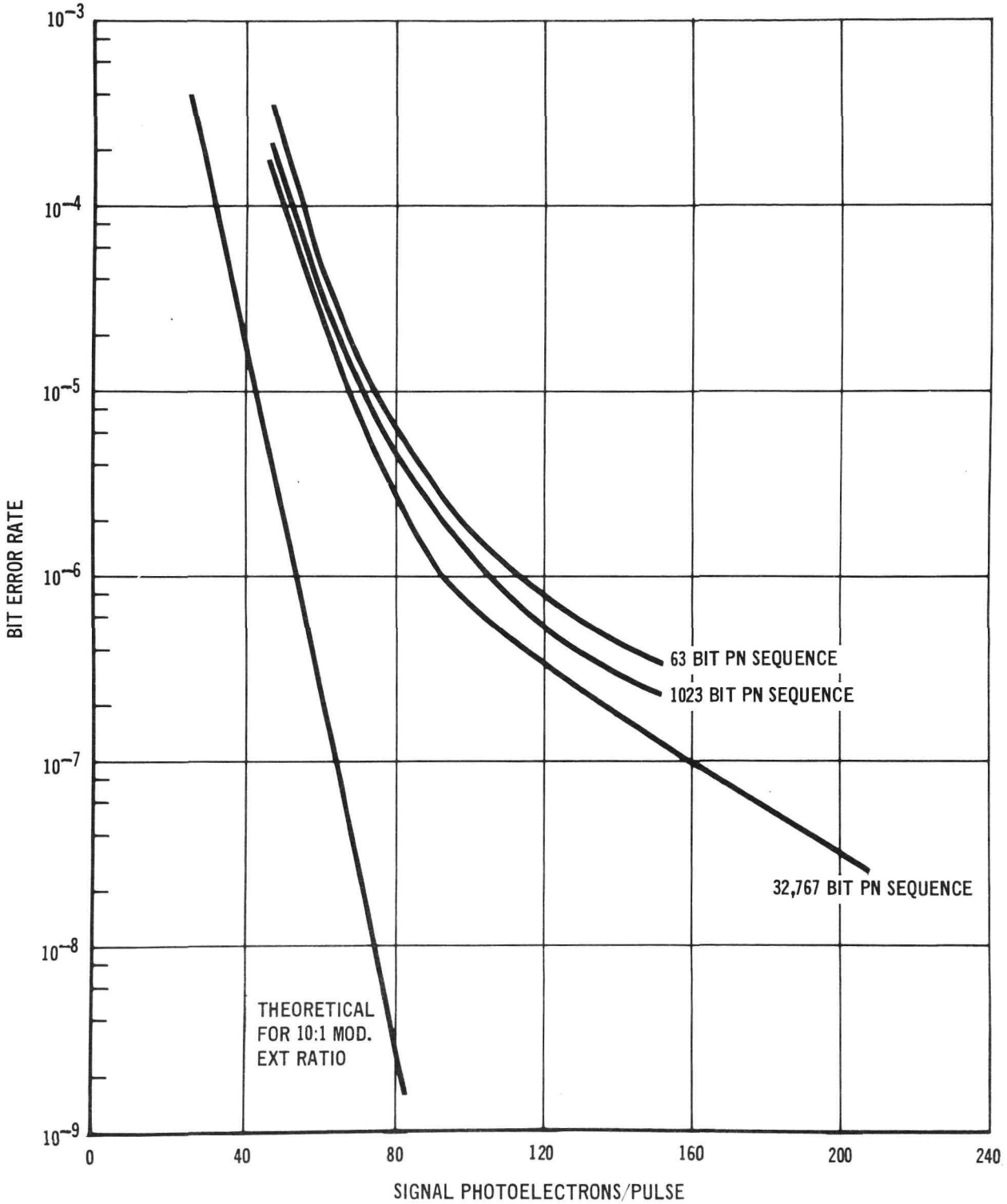


FIGURE 27 400 Mbps COMMUNICATION SYSTEM ERROR RATE DATA

7. ECOM DETECTOR

The 200 Mbps detector for ECOM is supplied with a 1.06 μm detector head. Differences between the ECOM detector and the NASA detector are discussed in detail. Operating instructions and performance test results for the ECOM detector are included in this section.

7.1 INTRODUCTION.

The ECOM detector is similar to the NASA detector in concept and design. The notable hardware differences are changes in the RF drive chain due to the lower bit rate and the larger, more powerful RF drive amplifier. There are also changes in the detector operating procedures and performance. Photos of the equipment are shown in Figures 28 and 29.

7.2 PERFORMANCE SUMMARY.

Measured performance results on the ECOM 1.06 μm Optical Detector are presented in Table 6.

TABLE 6

SUMMARY OF PERFORMANCE RESULTS

CHARACTERISTIC USING DCFP S/N 021	VALUE
Operating Wavelength (micrometers)	1.06
Photocathode Quantum Efficiency (maximum)	0.27%
Dynamic Range of Signal Input (photoelectrons per pulse)	100 to 1000
Required Input Laser Pulse Width	<500 picoseconds (at the 10% of maximum points)
Synchronization	
Acquisition Range at 200 Mbps	$\pm$ 25 kHz
Deviation Rate Product	$>1.6 \times 10^5$ Hz/sec
Acquisition Time (maximum)	1 sec
Loop Bandwidth	1 kHz
Clock/Data Timing Accuracy (picoseconds)	$\pm$ 50
Outputs	Two complementary outputs in NRZ format. Output levels are -800 mv and -1600 mv.

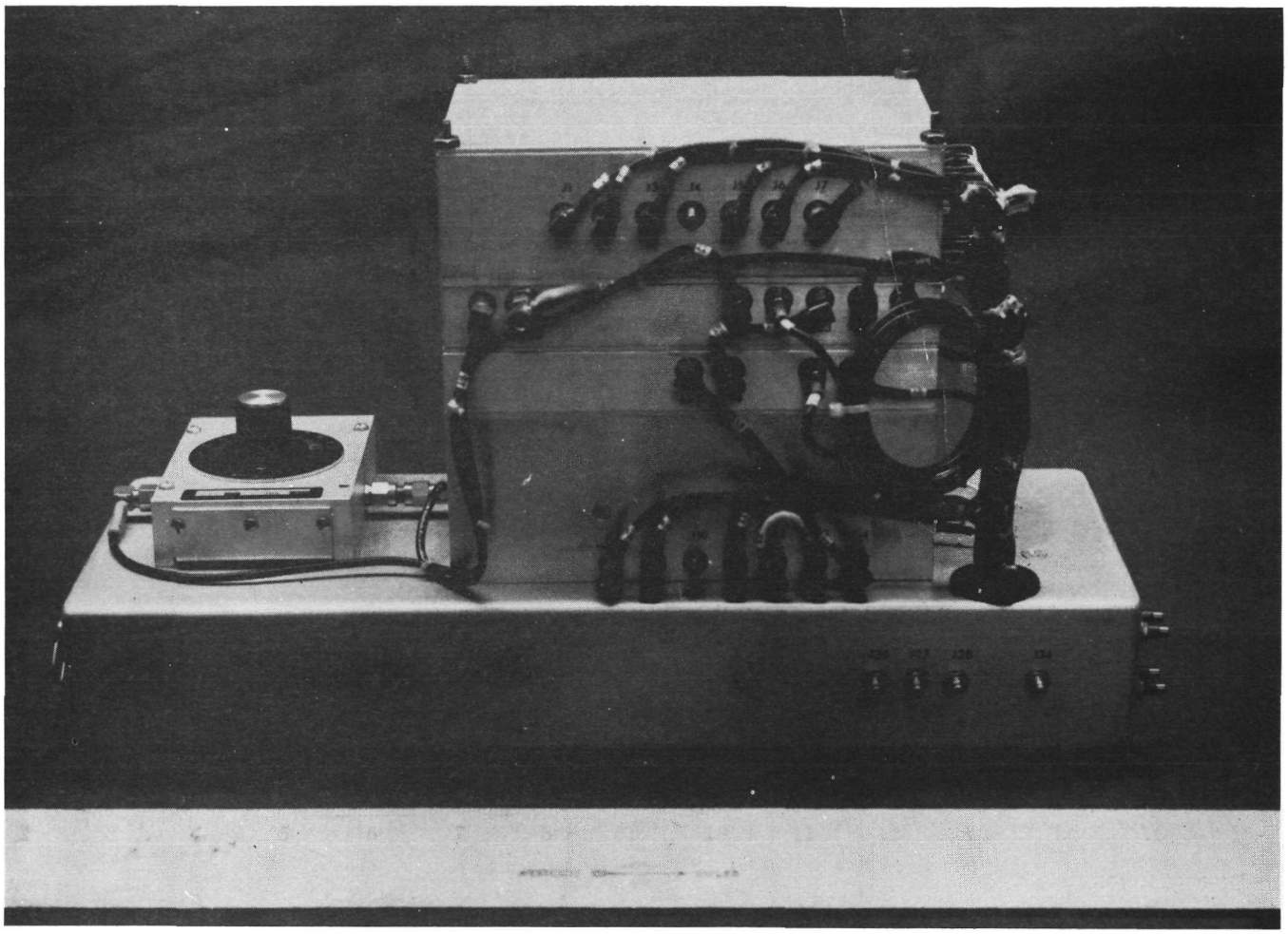


FIGURE 28 RECEIVER ELECTRONICS

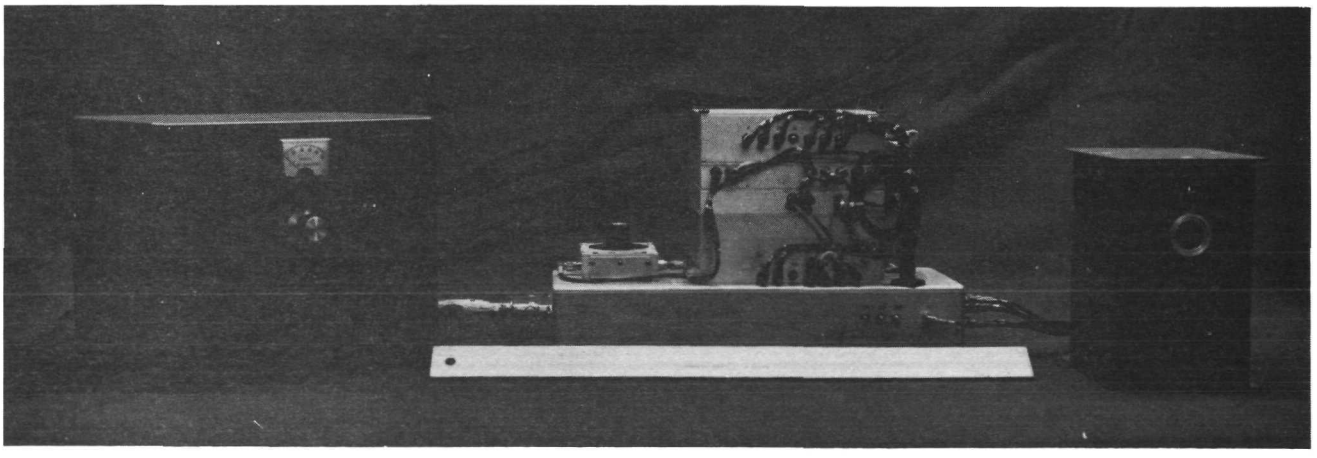


FIGURE 29 200 Mbps OPTICAL DETECTOR

7.3 HARDWARE DESCRIPTION.

A functional block diagram of the ECOM 200 Mbps Optical Detector is shown in Figure 30. This diagram is similar to that of the NASA detector in Figure 6 except that the RF drive electronics is reconfigured to allow external synchronization at the lower bit repetition frequency. A functional diagram of the RF drive electronics is shown in Figure 31. The clock synchronizer also operates at 200 MHz.

A larger, more powerful 1200 MHz power amplifier is used in the ECOM detector. This amplifier is less efficient and less expensive than the NASA unit which was optimized for size, weight, and power consumption. The power amplifier is located beneath a chassis which supports the remaining receiver electronics modules as shown in Figure 28. Some changes are incorporated in the automatic gain control circuitry to match the input characteristics of this amplifier.

7.4 OPERATING INSTRUCTIONS.

These procedures contain instructions for using the 200 Mbps receiver, indicating configuration definition for various operating modes, adjustment of various receiver operating parameters, specification of receiver interfaces and some measurement methods for evaluating receiver performance.

7.4.1 Initial Installation. The DCFP enclosure should be secured firmly to the optical table to insure mechanical stability. The control electronics power cable should be connected to the power and control unit, and 117 Vac 60 Hz applied to the ac power connector.

7.4.2 Input Beam.

7.4.2.1 Beam positioning. An optical method for adjusting the beam should be provided to allow for both vertical and horizontal displacement on the DCFP photocathode.

7.4.2.2 Beam size. The beam size at the photocathode should be as small as practical. Typical spot sizes used for testing the receiver are 0.20 mm to 0.25 mm diameter.

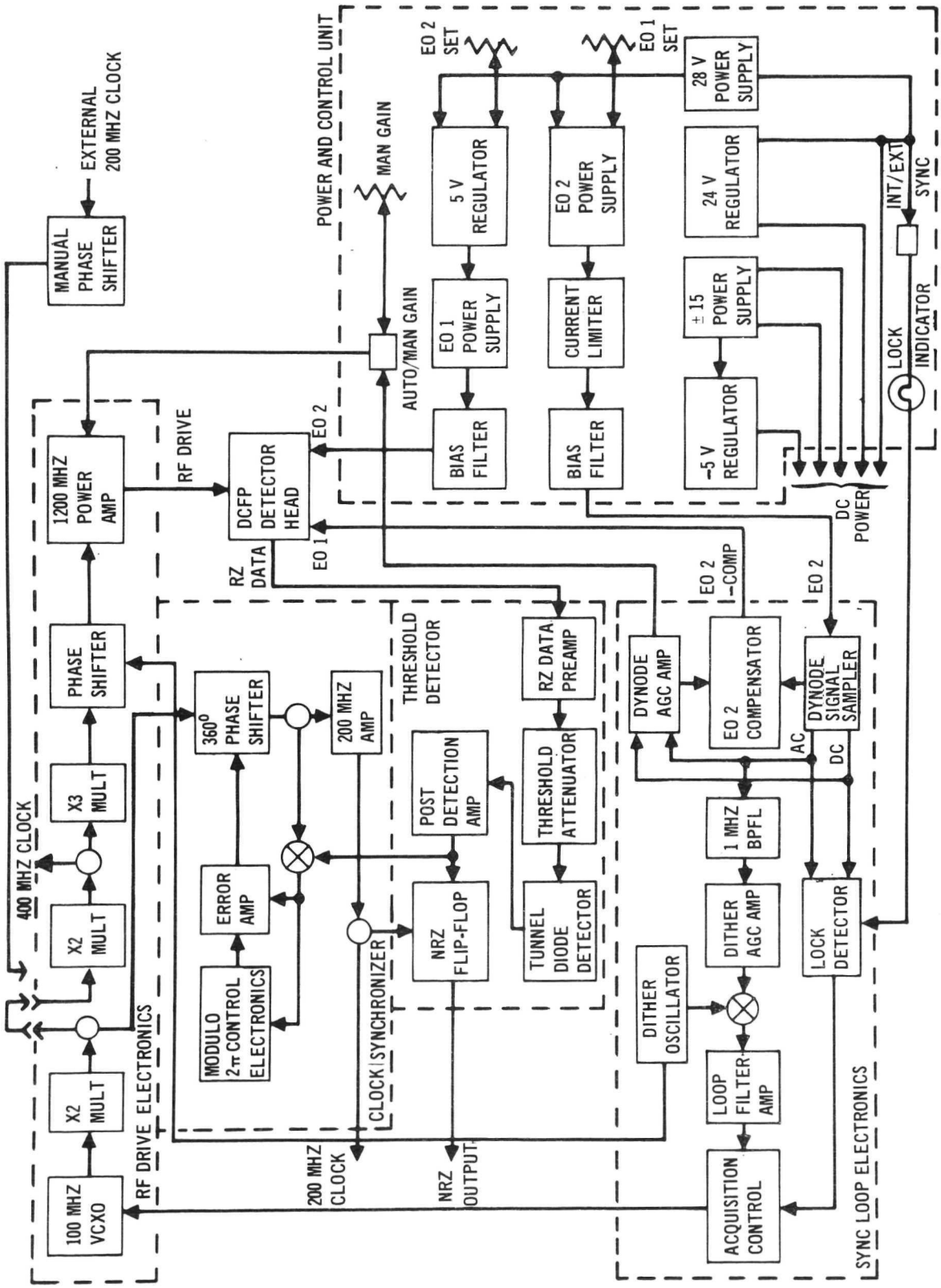


FIGURE 30 200 Mbps OPTICAL DETECTOR BLOCK DIAGRAM

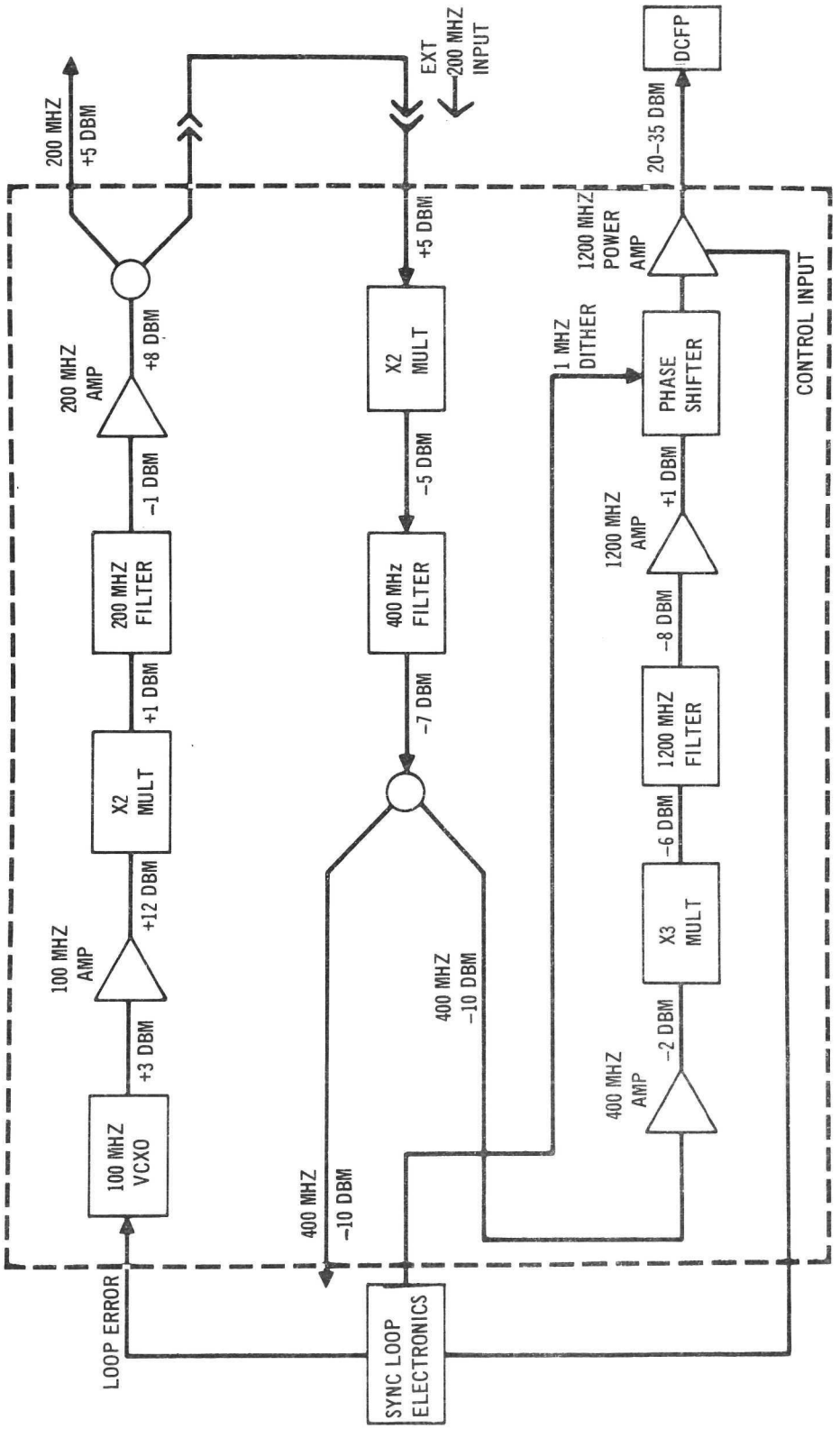


FIGURE 31 RF DRIVE ELECTRONICS FUNCTIONAL DIAGRAM (ECOM)

7.4.2.3 Beam intensity. The receiver is designed to work with optical signal levels corresponding to 30 photoelectrons/pulse to 1000 photoelectrons/pulse. At a quantum efficiency of 0.27% this corresponds to optical powers of 0.21 μW to 7.0 μW for a data rate of 200 Mbps (50% duty cycle). The absolute maximum optical power should not exceed 200 microwatts. Due to the higher quantum efficiency in the visible, no more than 2 microwatts of optical power should be applied.

7.4.3 DCFP Operating Parameters.

7.4.3.1 Dynode voltage adjustments. The static component of the electric field is provided by two independently adjustable high voltage supplies, one for each dynode. The two dynode biasing fields are designated E01 (dynode 1) and E02 (dynode 2). The adjustments for E01 and E02 are on the rear of the power and control unit. Also included are test jacks for monitoring the two dynode voltages. Caution should be used in measuring these voltages as they are typically -400 Vdc and a floating voltmeter must be used. E01 should be set at -450 Vdc and left at this value. The setting of E02 is dependent upon the desired receiver characteristics. The recommended value for E02 is -440 Vdc.

7.4.3.2 Magnetic field adjustments. The magnetic field should not require adjustment under normal receiver operation. However an adjustable screw is provided on each side of the detector head which allows the field to be varied. The number of turns from the full in position are calibrated in gauss as indicated in the calibration chart below. The normal setting is underlined.

TABLE 7

MAGNETIC FIELD CALIBRATION FOR DCFP S/N 021

TURNS FULL IN POSITION (Both Screws)	MAGNETIC FIELD GAUSS
0	320
1/2	330
1	340
1 1/2	355
2	370
3	380
4	390
5	400

7.4.3.3 RF interlock. The DCFP is provided with an interlock feature that prevents RF drive power from being applied unless both dynode voltages are adequate to prevent damage to the DCFP. The small circuit board within the mount provides this function. Switch S1 on this board allows for disconnecting the voltage sensing element from the first dynode. This should only be done when DCFP photocathode current is being measured. The "down" position for switch S1 is the photocurrent mode, and the "up" position is the normal operating position.

7.4.4 Synchronization Modes.

7.4.4.1 Internal (remote) synchronization. In this mode the receiver acquires synchronization from the input optical pulse train. The SYNC MODE switch on the control panel should be in the INT position and jumper cable P12-13 should be in place on the RF drive electronics. When the receiver is phase locked to the optical signal, the sync loop lock indicator will be illuminated.

7.4.4.2 External synchronization. The use of an external signal which is phase coherent with the optical pulses may be used to operate the receiver. This is accomplished by applying a 200 MHz signal to the manual phase shifter supplied with the receiver. The required level into the phase shifter is +5 dBm (1.1 Vp-p) ±1 dB. The output of the phase shifter is connected to J12 on the RF drive electronics in place of the jumper cable P12-13. The SYNC MODE switch should be in the EXT position for this mode of operation. The phase shifter is adjusted to center the DCFP gate on the optical pulse. This can be observed by monitoring the DCFP output with a sampling oscilloscope. If an NRZ data output is desired when operating in the EXT SYNC mode, an additional synchronous 200 MHz signal must be applied to the Clock Synchronizer input at J15. The level of this signal should be +5 dBm (1.1 Vp-p) ±1 dB and requires no external phase shifter.

7.4.5 Gain Control Modes.

7.4.5.1 Automatic gain control (AGC). The AGC mode is considered to be the normal operating mode for the detector. This mode is implemented by the DCFP gain switch being set to the AUTO position. When operating in the AGC mode, the optical signal may be varied without re-adjusting other receiver parameters. The meter on the control panel measures the DCFP second dynode current. Full scale for this meter is 100 μA. When operating in the AUTO mode, the AGC maintains the second dynode current constant at 50 μA over the receiver dynamic range. This value can be changed to any value from 50 μA to 200 μA by adjusting pot R45 on the Sync Loop Electronics Board. Since the AGC loop senses the average second dynode current, any long term change in data duty cycle will change the output pulse height correspondingly. This is normal.

7.4.5.2 Manual gain control. A manual gain control mode is also provided whereby the DCFP gain is varied by the MANUAL GAIN knob on the control panel. Before switching the DCFP gain switch to the MAN position the MANUAL GAIN control should be set to the extreme counterclockwise limit (minimum gain). The opposite convention is used in the NASA detector. Again the operating second dynode current is measured by the panel meter. An upper limit of

100 μA is recommended for long DCFP life. If the current exceeds 0.7 mA the current limiter in the second dynode power supply begins to reduce the bias voltage. A point is reached where the interaction of the current limiter and RF interlock results in an audible relay chatter in the power and control unit. This condition should not be allowed to remain for any period of time, as it represents an overload condition.

7.4.6 Threshold Detector.

7.4.6.1 Preamplifier input level. The data preamplifier in the Threshold Detector provides the necessary gain for the DCFP output levels to the tunnel diode operating levels. It is essential that this amplifier be operated in its linear region, so the input level must be attenuated to the extent that the preamp output level at J21 is approximately 400 mV peak-to-peak. The DCFP output pulse amplitude will vary depending on the number of gain steps selected by varying E02, the dynode current, and the duty cycle of the digital data. A 3 dB or 6 dB pad in the input line should be used if the level at J21 exceeds 400 mV.

7.4.6.2 Threshold attenuator setting. The variable attenuator on the receiver mounting plate provides the means of adjusting the amplitude of the pulse going to the tunnel diode threshold detector. The optimum setting for this attenuator is dependent on optical signal power and preamplifier output level. To set it properly, the NRZ data output should be monitored at J24 either with error rate instrumentation or a sampling oscilloscope. The former method is much more sensitive and is therefore preferred.

7.4.7 Receiver Outputs.

7.4.7.1 NRZ data output. Complimentary NRZ data outputs are provided at J27 and J28. The levels are standard MECL levels of -800 mV and -1600 mV.

7.4.7.2 Synchronous clock output. A 200 MHz clock is available at J18. This clock is always synchronous with and maintains the same phase relationship with the NRZ data. The amplitude of this clock is nominally +4 dBm into a 50 ohm load.

7.4.7.3 400 MHz clock. A -10 dBm 400 MHz clock is available at J10 of the RF drive electronics when operating in the internal synchronization mode.

7.4.8 DCFP Photocurrent/Quantum Efficiency Measurement. To measure the DCFP photocathode current, observe the following procedure.

(1) Turn off power to the receiver.

(2) Disconnect P31 from J31.

(3) Remove DCFP enclosure cover. Move interlock switch S1 in the DCFP enclosure to the DOWN position.

(4) Place magnetic field shorting plate into position inside the DCFP assembly.

(5) Connect a 300 volt battery and nanoammeter to P31 as shown in Figure 15.

(6) Reduce ambient light as much as possible.

(7) Measure the cathode current with and without presence of the 1.06 μm optical beam. The difference is the photocurrent.

(8) Measure the incident power of the optical beam.

(9) Compute photocathode yield = $\frac{\text{photocurrent}}{\text{optical power}}$ in amps/watt.

Multiply by $\frac{100\%}{0.86 \frac{\text{amps}}{\text{watts}}}$ to obtain the quantum efficiency in percent.

7.5 PERFORMANCE TESTS.

This section discusses the performance tests applied to the ECOM optical detector.

7.5.1 Gain Characteristics. The DCFP was operated in a special test set up in which fixed operating biases were maintained at preset levels. The RF drive was derived directly from the laser transmitter output rather than

using the remote synchronization circuitry. Input photocathode current in response to the laser transmitter signal was calibrated against a precision variable optical attenuator placed in the optical beam. Anode output current was then plotted versus input current at various RF drive power levels. The dc dynode bias was adjusted slightly to compensate for step size variations with RF drive level. The resultant transfer characteristics for DCFP S/N 021 are presented in Figure 32. The number of steps is the same for each power level. The linearity of these curves is excellent up to 100 μA of second dynode current.

7.5.2 Quantum Efficiency. The photocathode quantum efficiency of the DCFP was determined by measuring the photocurrent due to a known optical signal level. DCFP photocurrent was measured by operating the DCFP as a photodiode, with magnetic field and RF drive power removed. With only the dc electric field bias acting on the photoelectrons, they were accelerated to and collected by the rail electrode which was at ground potential. The cathode response in amps per watt was compared with the theoretical maximum of one electron per photon, which is 0.86 amps per watt at 1.06 μm, in order to determine the quantum efficiency.

The quantum efficiency of DCFP S/N 021 at 1.06 μm was 0.17% average and had a hot spot of 0.27%.

The quantum efficiency of DCFP S/N 021 at 0.53 μm was about 3.5% average and had a hot spot of 5.3%.

7.5.3 Collector Efficiency. The collector efficiency is the portion of the second dynode current which is delivered to the anode and is a function of the DCFP operating conditions. At lower gain and fewer multiplication steps, the phase focusing and bunching is tighter, and a greater fraction of the dynode current passes through the collector aperture to reach the anode. The chosen operating conditions for DCFP S/N 021 result in a collector efficiency greater than 17% over the operating range.

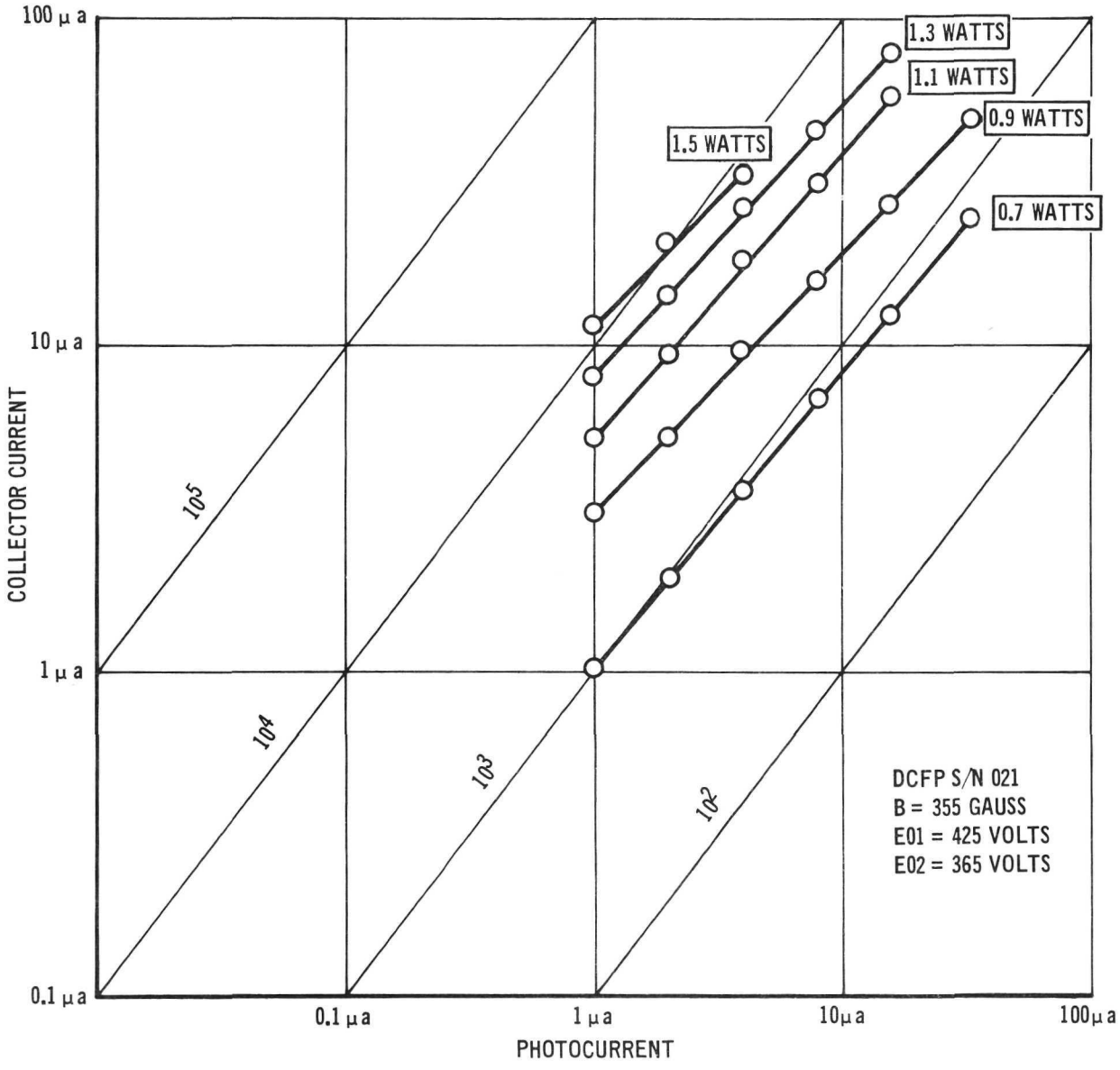


FIGURE 32 DCFP S/N 021 CURRENT GAIN

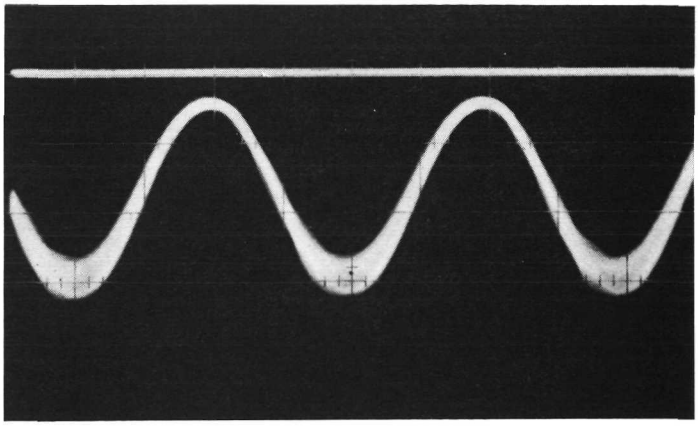
7.5.4 Gating. Gating is measured by a convolution technique in which the narrow mode locked laser pulses are used to sample the shape of the DCFP gating function. The DCFP gating function is synchronous with the RF drive. The RF drive frequency is chosen to be slightly different than the frequency of the incoming optical pulse train. Each succeeding pulse is then received at a different portion of the DCFP gating function which in turn affects output pulse amplitudes corresponding to the degree of gating. The envelope of the output pulse train then reproduces the shape of the gating function at the difference frequency to an accuracy limited by the laser pulse width. If the DCFP output is displayed on a low frequency oscilloscope, integration of this output pulse train results in a display of the envelope which is the convolution of the optical pulse train with the DCFP gating function.

The convolution waveform of DCFP S/N 021 with normal operating bias is shown in Figure 33 in response to a 200 Mpps mode locked laser pulse train. Unfortunately, the sampling laser pulse is too wide to allow an accurate determination of gate width.

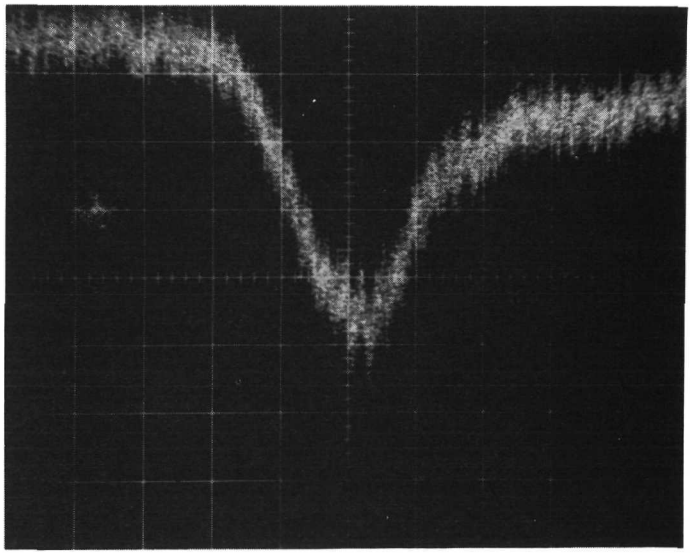
7.5.5 Acquisition and Synchronization. Tests of the acquisition and synchronization functions were designed to measure the static and dynamic limits of loop performance.

To measure the static acquisition range, the frequency of the 200 Mpps mode locked laser was offset until acquisition was no longer achieved. At 50 photoelectrons/pulse the static acquisition range was ±25 kHz.

The dynamic performance of the synchronization loop is described by the deviation-rate product. This figure was measured by frequency modulating the test laser with a triangular modulating waveform at a peak deviation of ±.83 kHz and slowly increasing the modulation frequency until the loop lost lock. The allowed transmitter deviation-rate product is 3.3×10^5 Hz/sec at 1000 photoelectrons per pulse and decreases to 1.7×10^5 Hz/sec for input signals down to 30 photoelectrons per pulse, as shown in Figure 34.



NORMAL OPERATION
E01 = 450 VOLTS
E02 = 388 VOLTS
B = 370 GAUSS
ESTIMATED GATE WIDTH
IS 200 TO 250 PSEC AT
50% OF MAXIMUM



SAMPLING LASER PULSE
WIDTH = 440 PSEC
AT 50% OF MAXIMUM
HORIZONTAL = 200 PSEC/DIV

FIGURE 33 CONVOLUTION OF DCFP S/N 021 GATING FUNCTION

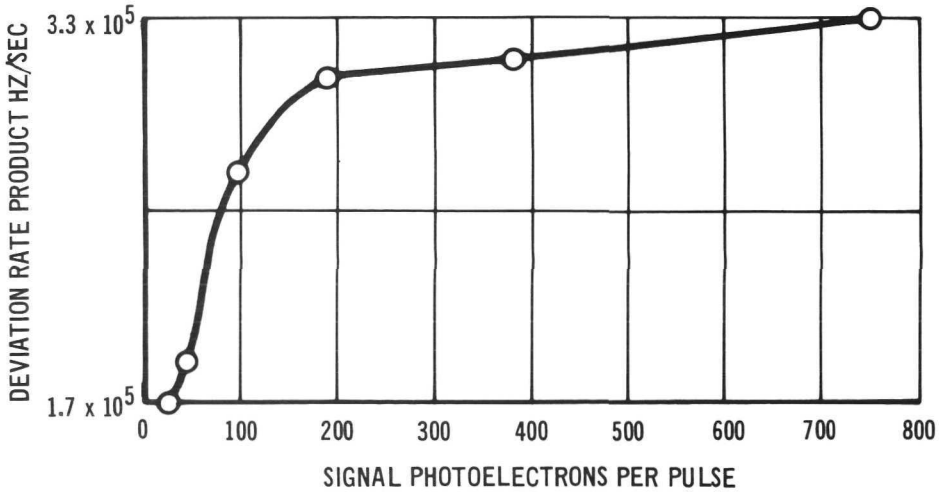


FIGURE 34 SYNCHRONIZATION LOOP DYNAMIC TRACKING CAPABILITY

The loop bandwidth and damping factor were estimated at 1 kHz and 0.7 respectively using a similar test at lower deviation with a sinusoidal modulating signal.

7.5.6 RF Drive Chain. The spectral purity of the RF drive chain outputs at 200 MHz, 400 MHz and 1200 MHz is similar to that displayed for the NASA detector in Figure 19, though the levels are somewhat different. The 1200 MHz drive to the DCFP is variable up to 1.2 watts.

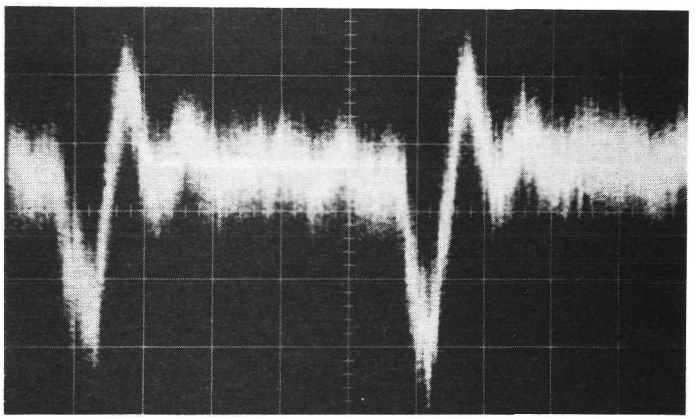
7.5.7 Automatic Gain Control. The characteristics of the dynode AGC loop were specified by static error of the dynode current and illustrated by photographs of the output pulse amplitude of the DCFP detector.

The static error was a measure of the change in dynode current as the optical input signal was varied. Decreased loop gain in this detector allowed a static error of ±12% over the range of 50 to 800 photoelectrons per pulse.

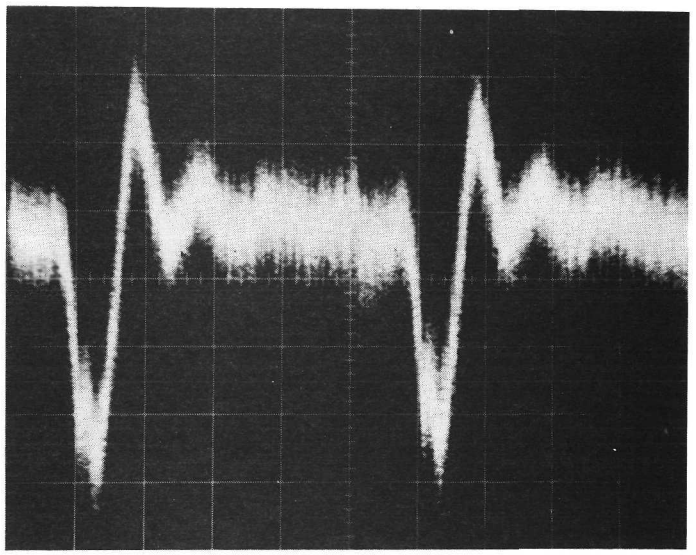
The effect of AGC and E02 bias compensation on the detector output pulse is shown in Figure 35. These photographs demonstrate that the receiver had a dynamic range of input optical power greater than 10 dB (corresponding to a 20 dB range of detected photocurrent). The different E02 voltages indicate the amount of bias compensation required to change step size to keep the output pulse centered in the dynode collector aperture.

7.5.8 Threshold Detector. Following is a summary of measured characteristics of the Threshold Detector:

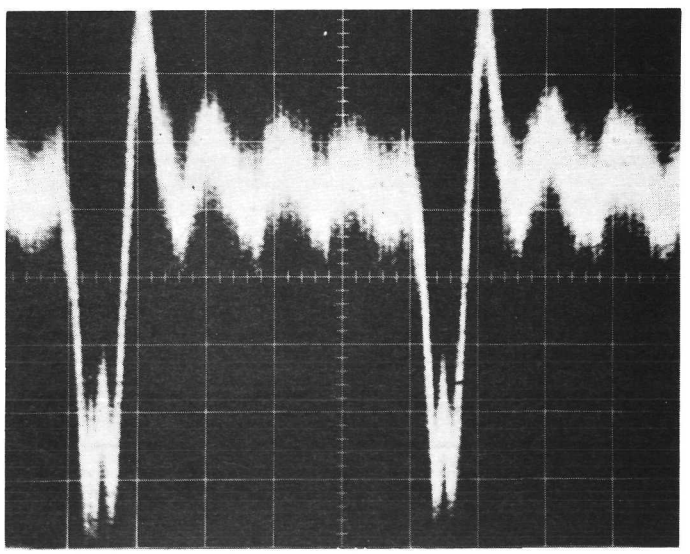
Preamplifier Bandwidth	dc - 600 MHz ±1.5 dB
Preamplifier Gain	100
RZ Input Range	10 - 20 mV peak
Threshold Resolution	1 dB
Post Detection Amplifier Bandwidth	dc - 700 MHz ±1.5 dB
Post Detector Amplifier Gain	10
NRZ Output Levels	-800 mV and -1600 mV



30 PHOTOELECTRONS/PULSE



90 PHOTOELECTRONS/PULSE



300 PHOTOELECTRONS/PULSE

VERTICAL 2 mV/DIV
HORIZONTAL 1 nS/DIV
E01 = 450 VOLTS
E02 = 370 TO 385 VOLTS
B = 370 GAUSS
Id_2 = 50 μ a

FIGURE 35 DCFP S/N 021 OUTPUT WITH AGC

Figure 36 includes various threshold detector waveforms. Figure 36A shows the preamplifier output. Figure 36B shows the output of the tunnel diode threshold detector and post detection amplifier for the same input signal. Figure 36C is the clock/data relationship which was required at the NRZ data output. Figure 36D is the NRZ data output.

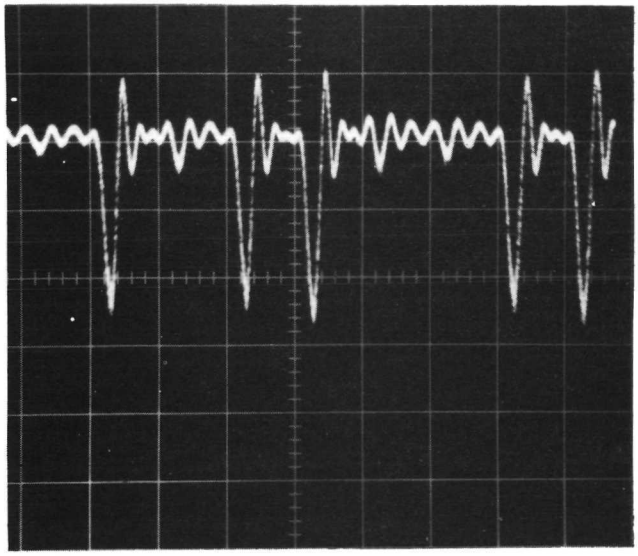
7.5.9 Clock Synchronizer. The essential requirement for the clock synchronizer is to keep the clock phase fixed with respect to the data. The second order control loop had the following measured parameters:

Closed Loop Gain	65
Closed Loop -3 dB Bandwidth	40 kHz
Static Phase Error	±6° maximum

These closed loop parameters were measured by electronically phase shifting the clock input signal to the clock synchronizer. The bandwidth was measured by phase modulating the clock signal with a variable frequency sine wave. The static phase tracking error is similar to that shown in Figure 22 as a function of phase difference between the clock and data signals. The worst case static error of ±6° corresponded to a timing error of ±42 picoseconds at the input to the NRZ conversion flip-flop. This was well within the requirement of ±80 ps for proper flip-flop operation.

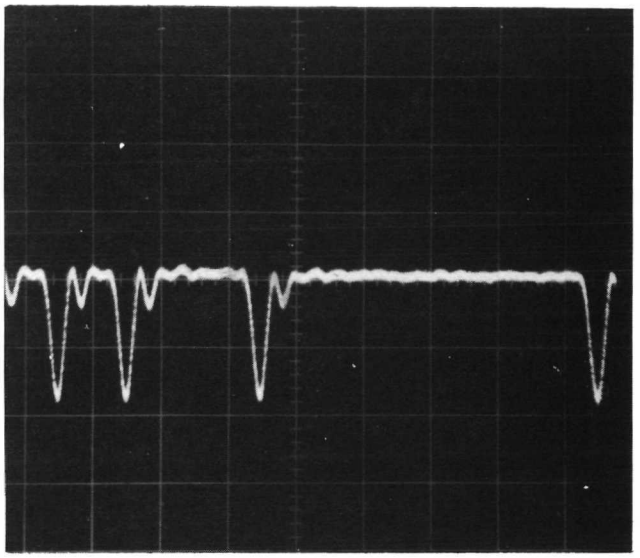
7.5.10 Dark Anode Current. At high gain, DCFP S/N 021 demonstrates a large dark anode current which is not due to dark cathode current. Cooling tests have revealed a strong temperature dependence of the dark anode current which indicates that it is due to thermionic emission on the first dynode prior to the cathode. These thermionic electrons undergo one or two gain steps before reaching the cathode and two additional steps of very high gain on the cathode where they compete with the signal photoelectrons for a portion of the output current. Due to the additional gain steps, the thermionic dark anode current increases much more rapidly than the signal with increasing RF drive power. Improvements will be incorporated into future DCFP's to eliminate this problem.

The output dark current of DCFP S/N 021 reaches a level of 20 μa at the second dynode when the overall gain is 5×10^3 and the RF drive power is 1.2 watts. The DCFP in the ECOM receiver is operated at the lowest possible gain



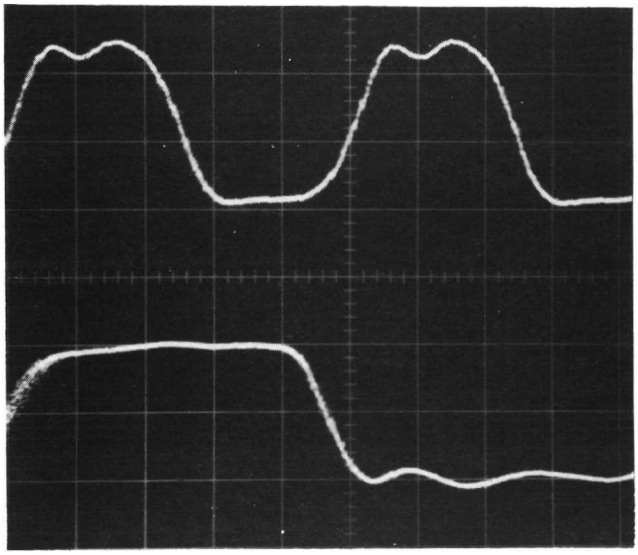
A

PREAMPLIFIER OUTPUT
400 mV/DIV, 5 nSEC/DIV



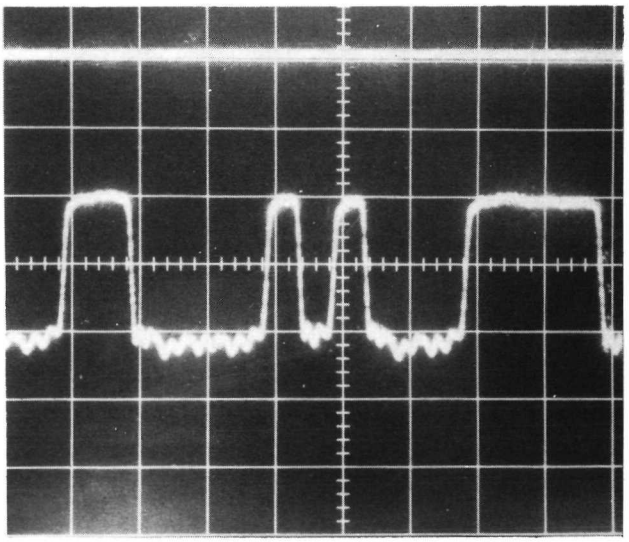
B

POSTAMPLIFIER OUTPUT
500 mV/DIV, 5 nSEC/DIV



C

(upper) CLOCK
(lower) NRZ DATA OUT
400 mV/DIV, 1 nSEC/DIV



D

NRZ DATA OUT
400 mV/DIV, 10 nSEC/DIV

FIGURE 36 200 Mbps THRESHOLD DETECTOR WAVEFORMS

in order to minimize the effects of the dark current. Reserve gain in the following preamplifier is utilized to bring the signal up to the required level for threshold detection.

8. CONCLUSIONS

At the conclusion of this program, a 400 Mbps Gated High Speed Optical Detector was delivered to NASA GSFC. This equipment is a highly efficient detector of binary encoded 400 Mpps mode locked laser pulses. Error rate measurements performed with this detector, the associated error rate electronics, a 400 Mpps mode locked and frequency doubled Nd:YAG laser, and an electrooptic modulator driven by pseudorandom codes have demonstrated very good overall system performance. Similar measurements under other programs have attributed only 1/2 to 1 dB of system degradation to the DCFP and the remainder to limitations of the electrooptic modulator and the electronics, and instabilities in the laser.

A similar 200 Mbps detector was delivered to Army ECOM, Fort Monmouth.